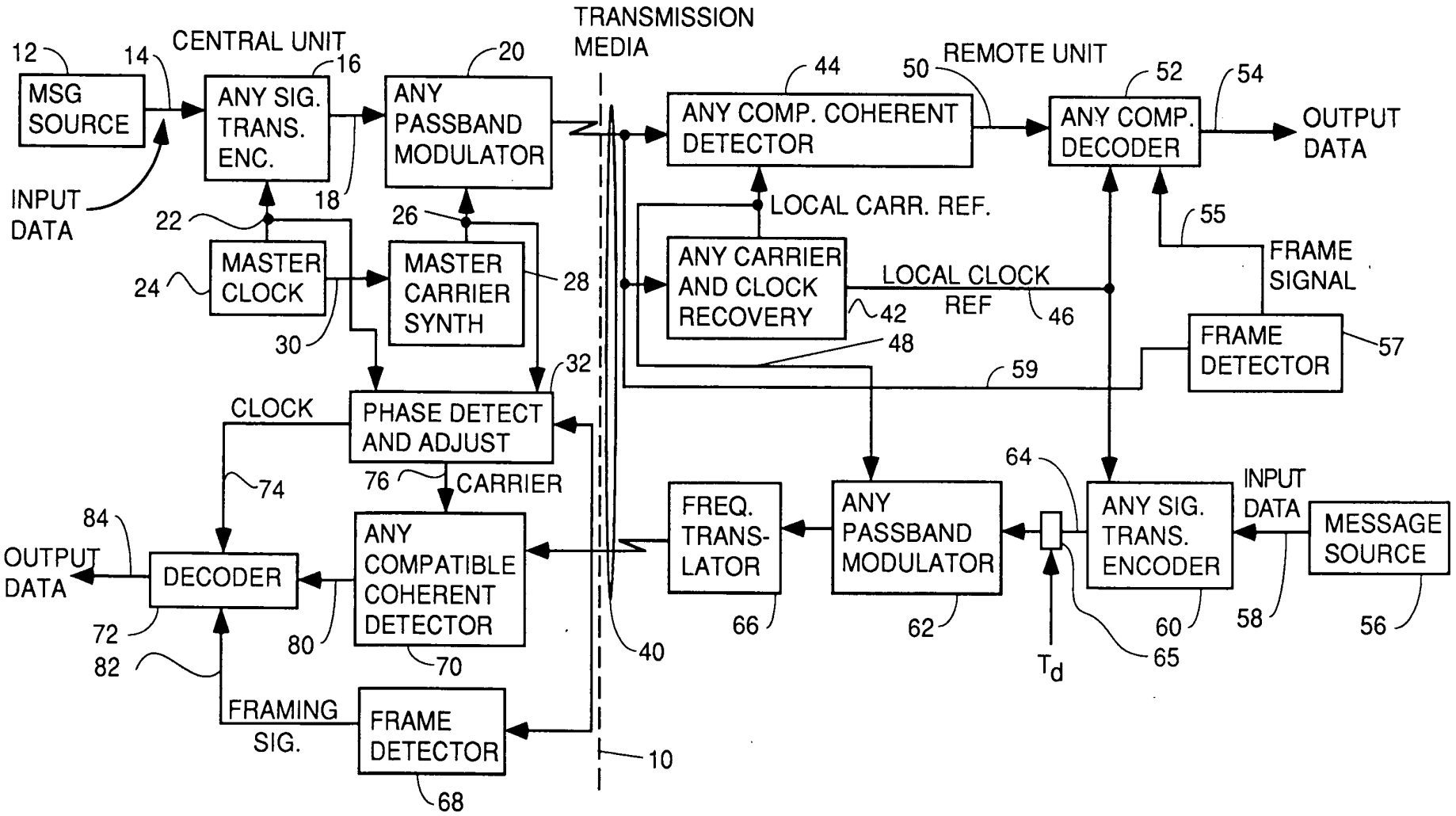
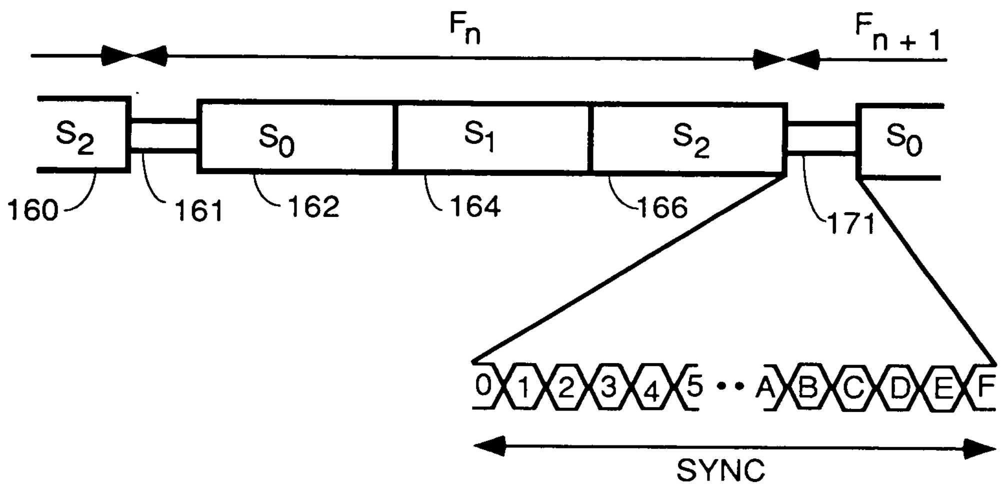
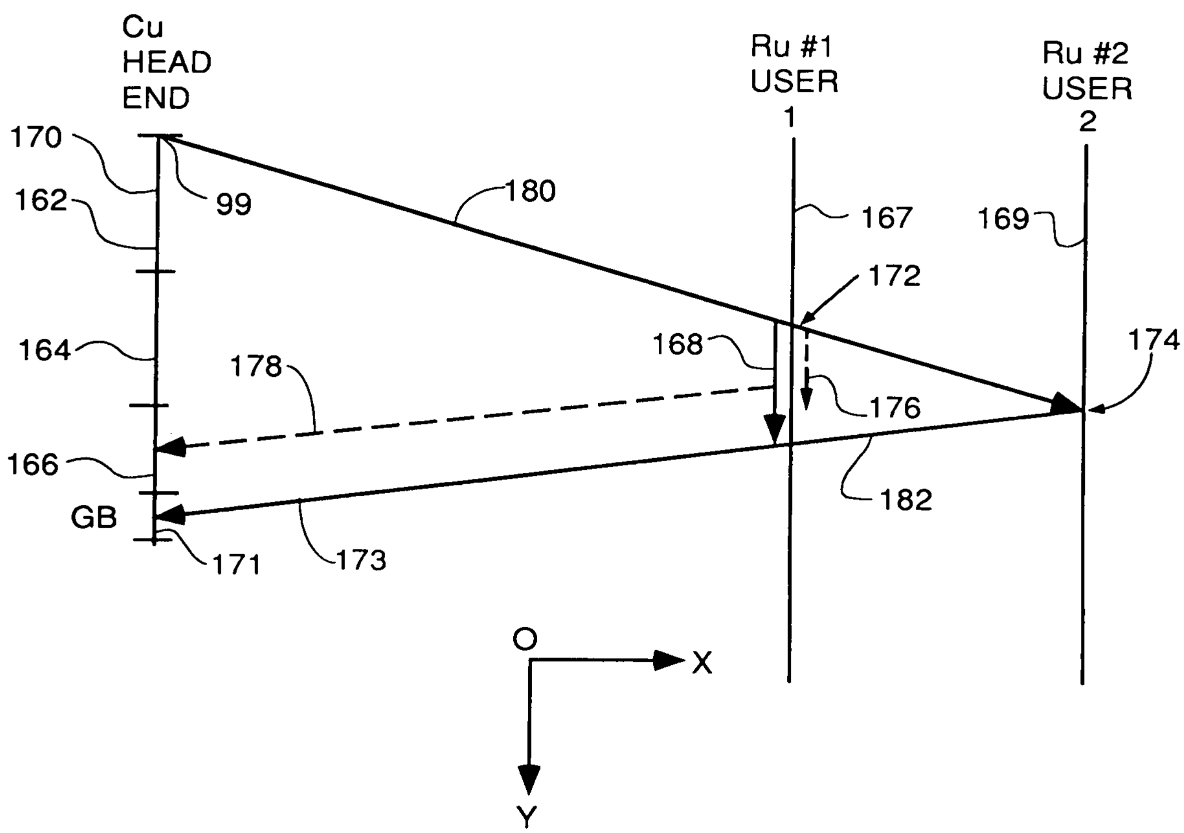


FIG. 1



F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 •• A B C D E F
SYNC

FIG. 2A



Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
99
180
167
169
172
164
178
168
174
176
166
182
GB
171
173
O
X
Y

FIG. 2B

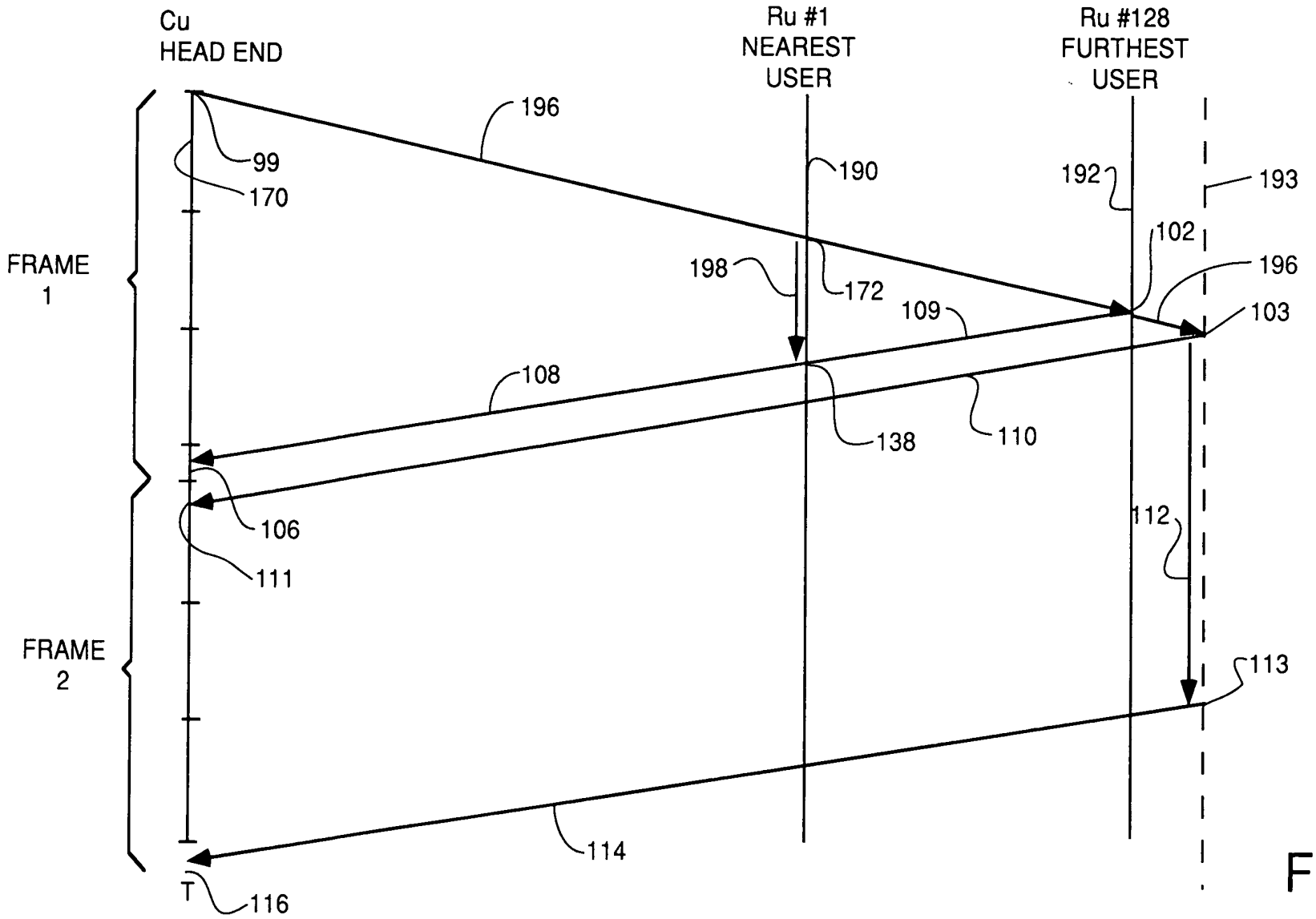


FIG. 3

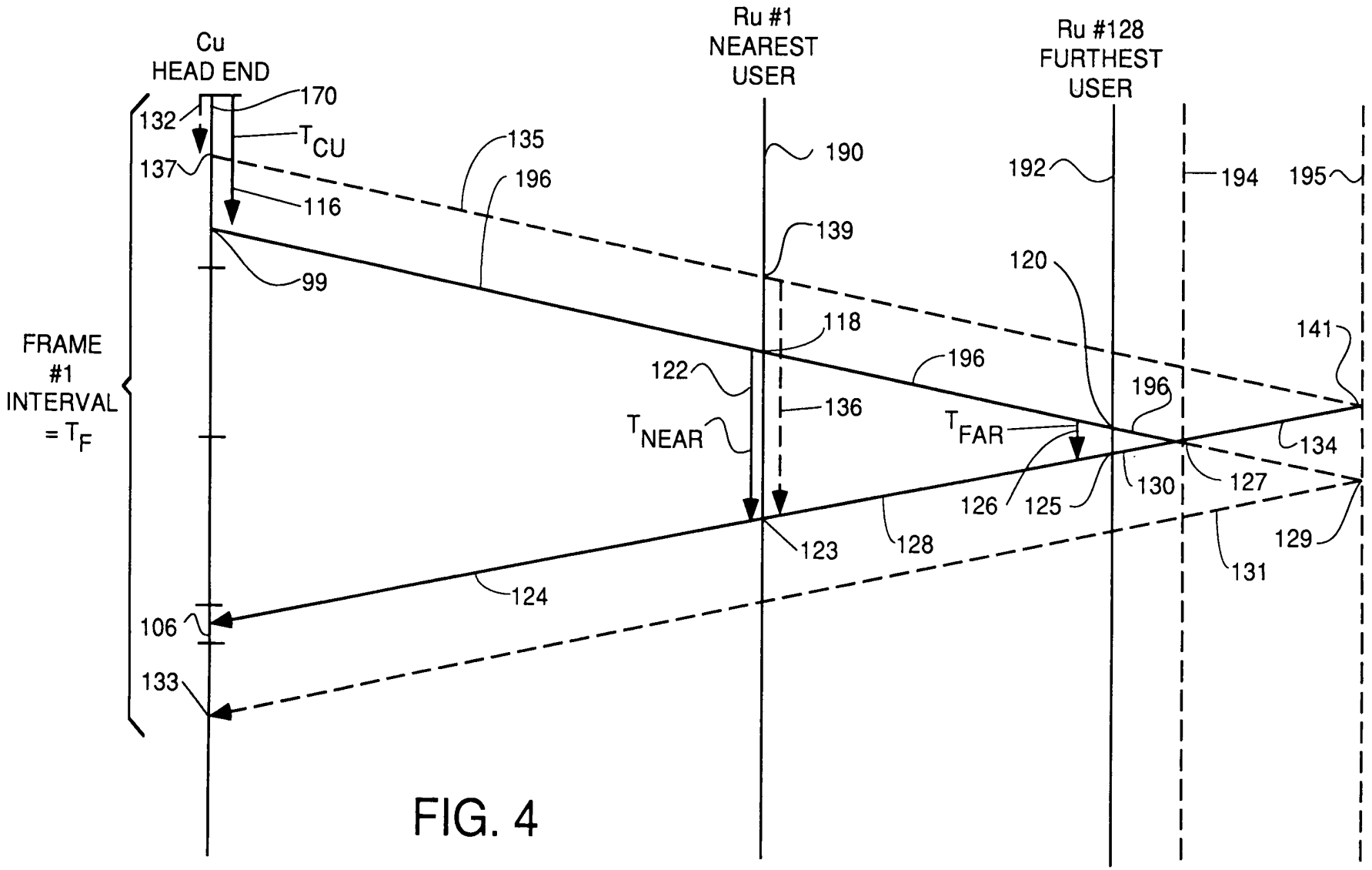
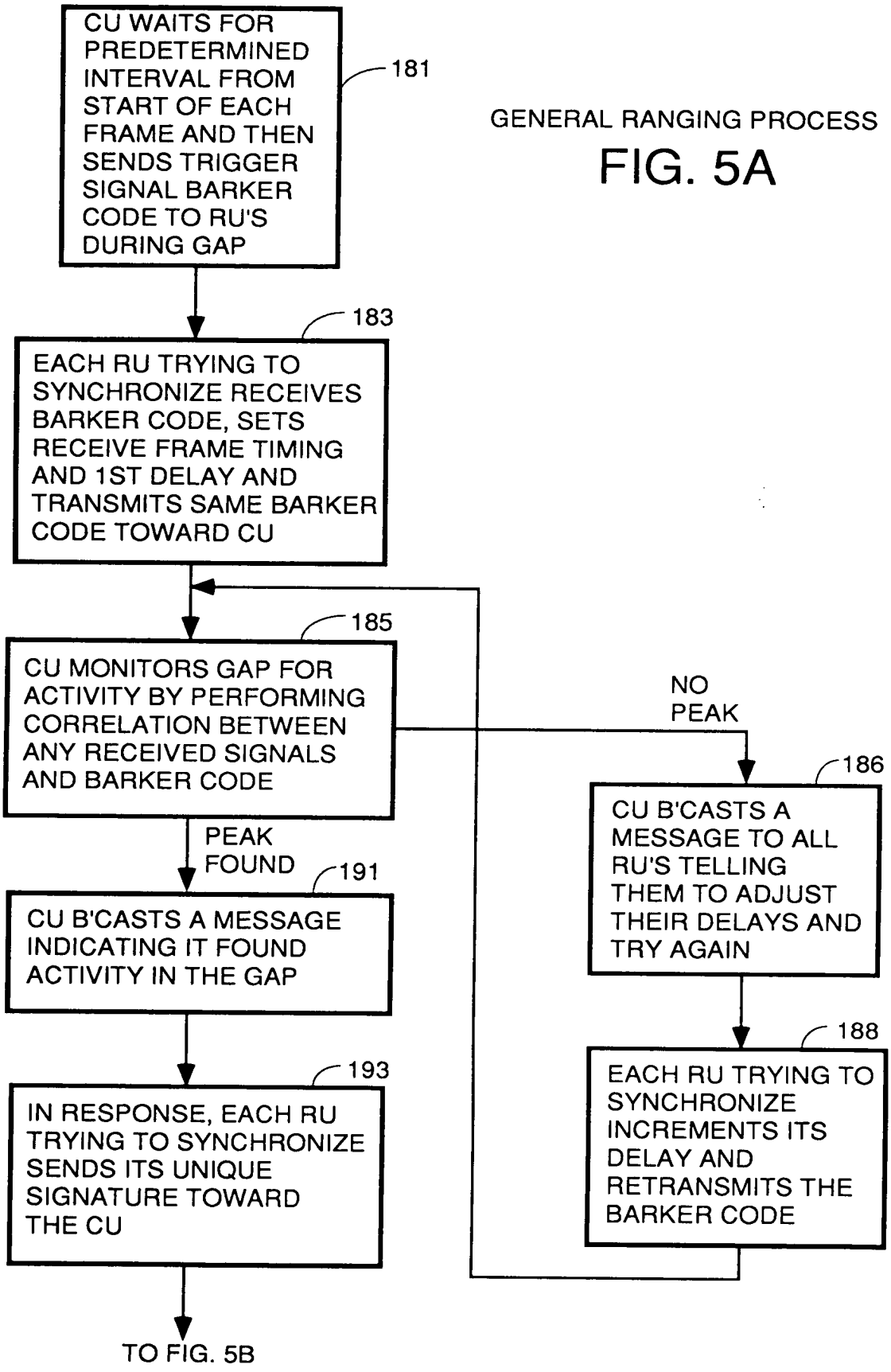


FIG. 4



GENERAL RANGING PROCESS

FIG. 5A

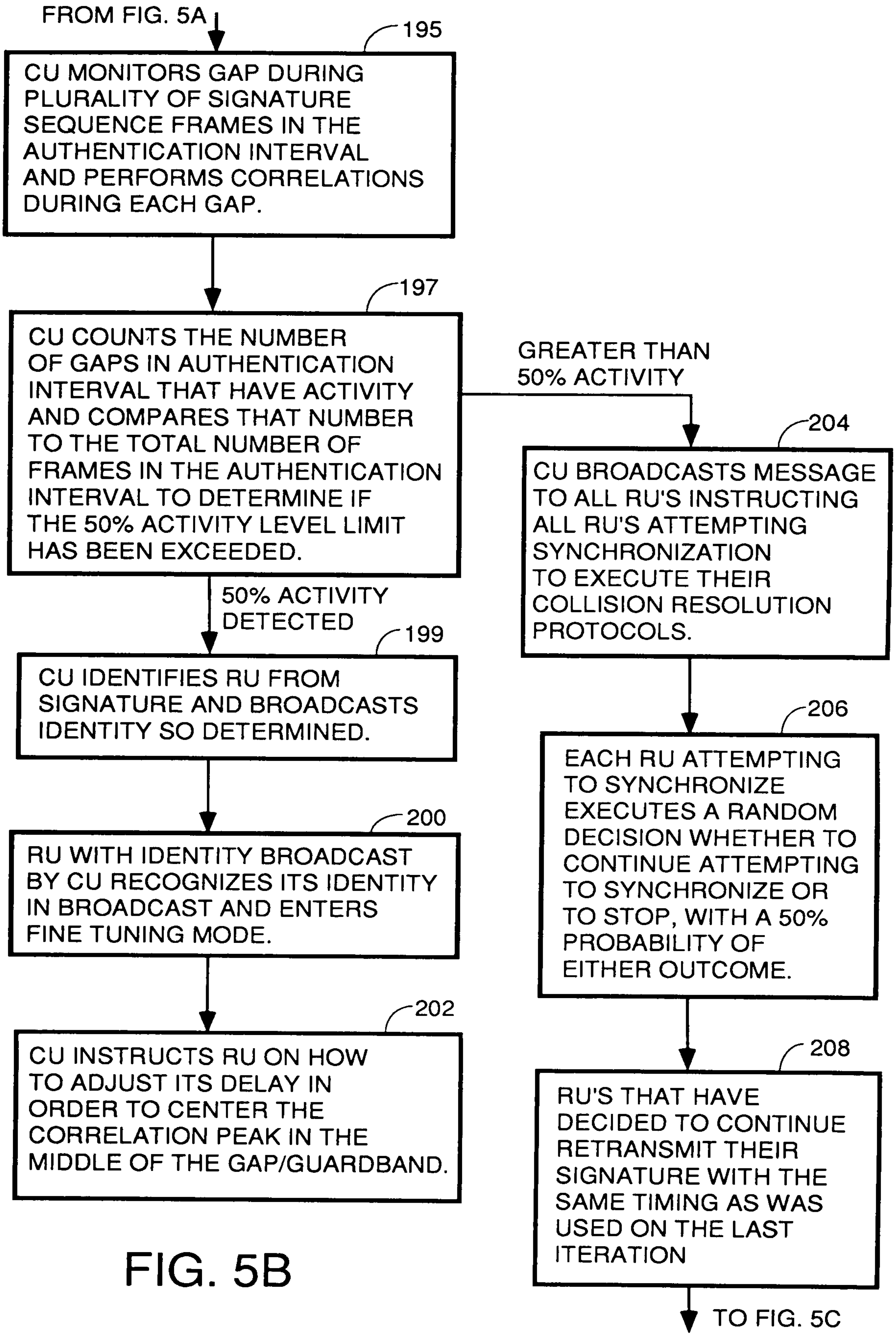

FROM FIG. 5A
195
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
50% ACTIVITY DETECTED
199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C

FIG. 5B

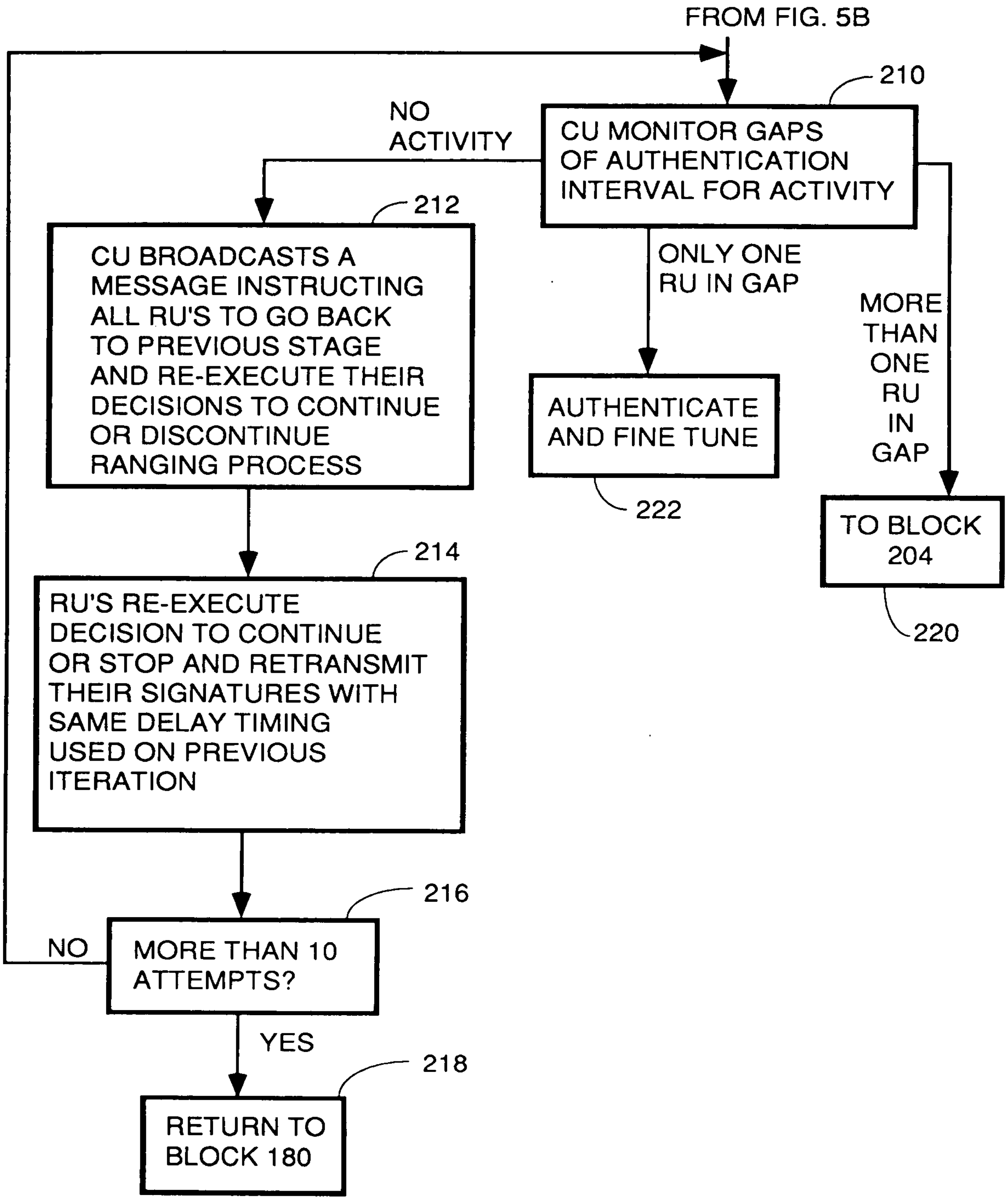

FROM FIG. 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C

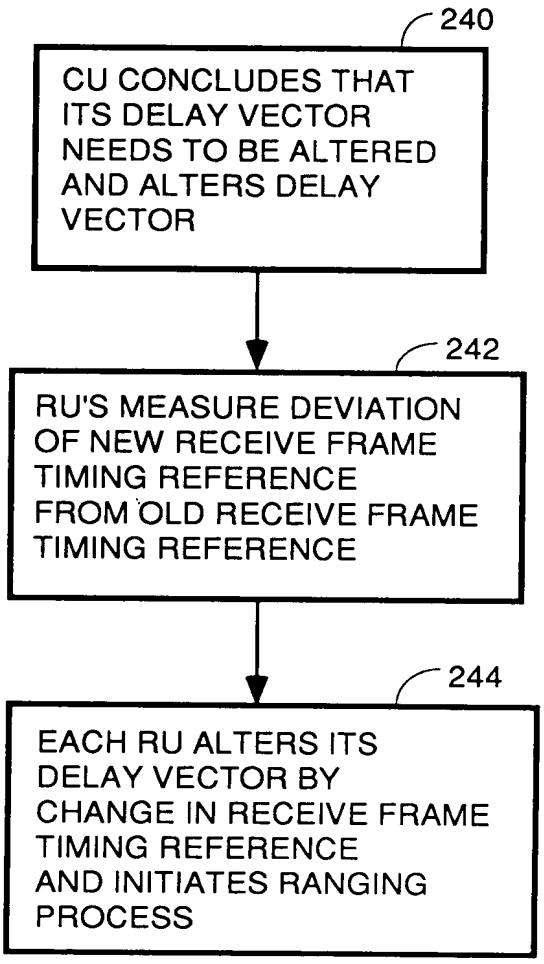


FIG. 6
DEAD RECKONING RE-SYNC

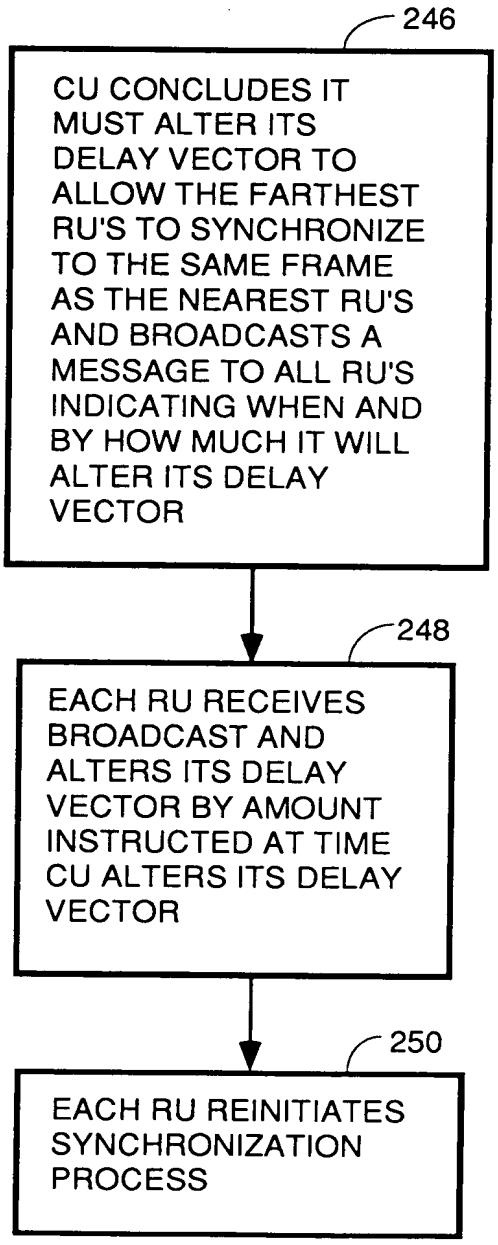
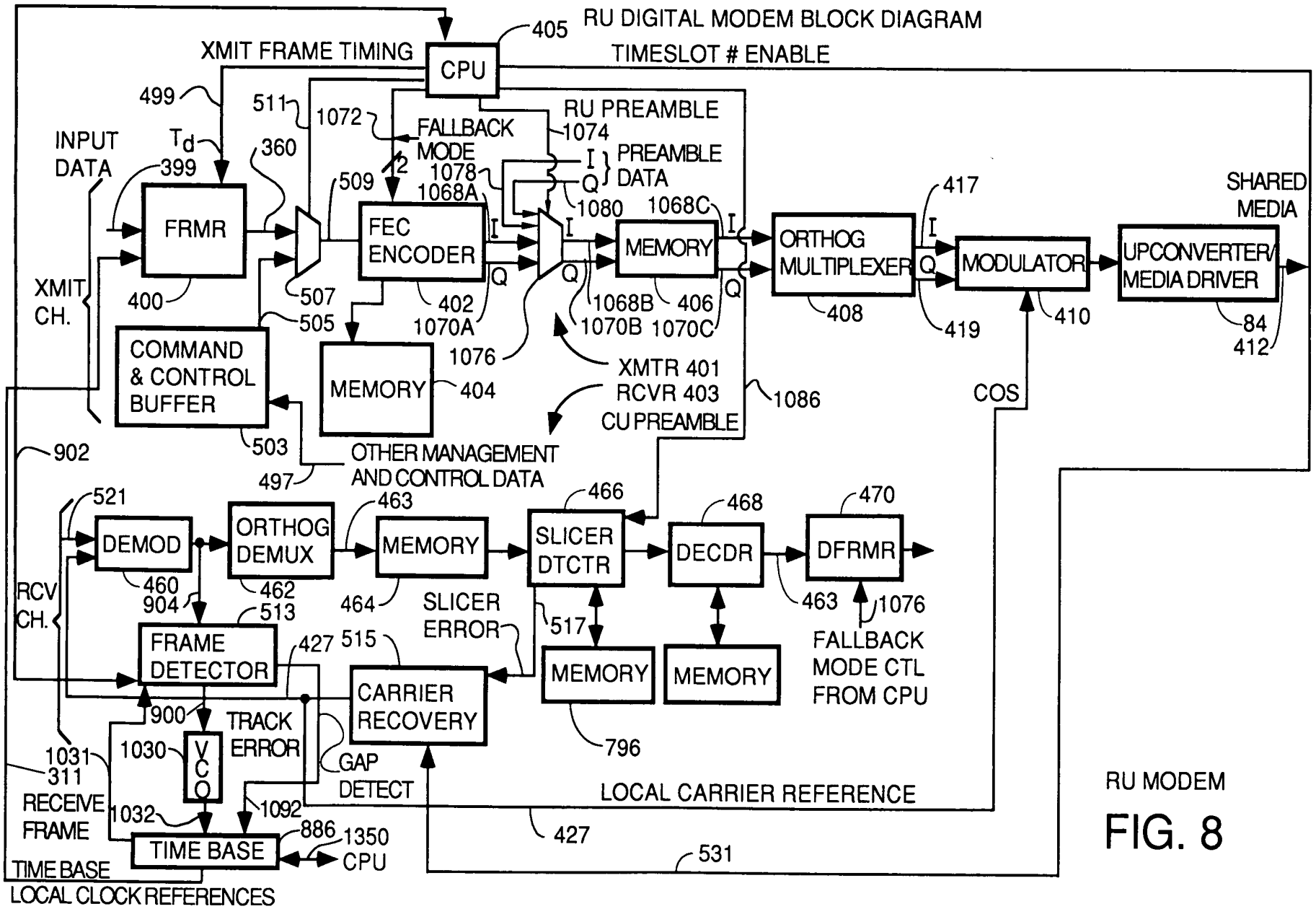


FIG. 7
PRECURSOR EMBODIMENT



RU MODEM

FIG. 8

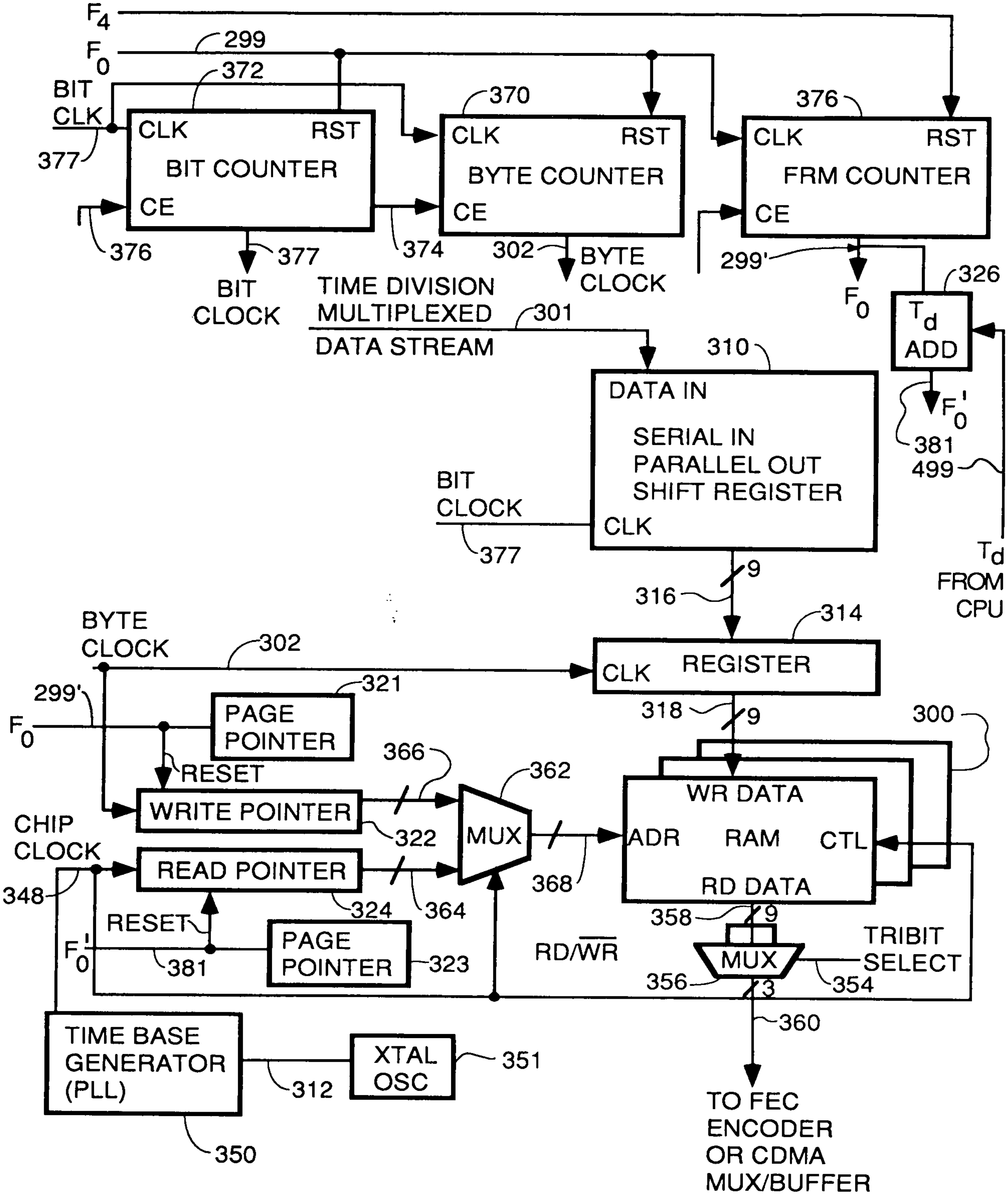

F4
F0
299
372
BIT CLK
377
370
376
CLK
RST
BIT COUNTER
CE
BYTE COUNTER
FRM COUNTER
376
377
374
302
BYTE CLOCK
299'
F0
326
Td ADD
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
F0'
381
499
BIT CLOCK
377
Td FROM CPU
9
316
314
BYTE CLOCK
302
REGISTER
321
299'
F0
PAGE POINTER
318
300
366
RESET
362
WRITE POINTER
WR DATA
CHIP CLOCK
322
MUX
ADR
RAM
CTL
READ POINTER
368
RD DATA
348
324
364
358
RESET
F0'
PAGE POINTER
323
RD/WR
TRIBIT SELECT
381
356
354
3
360
TIME BASE GENERATOR (PLL)
XTAL OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 9

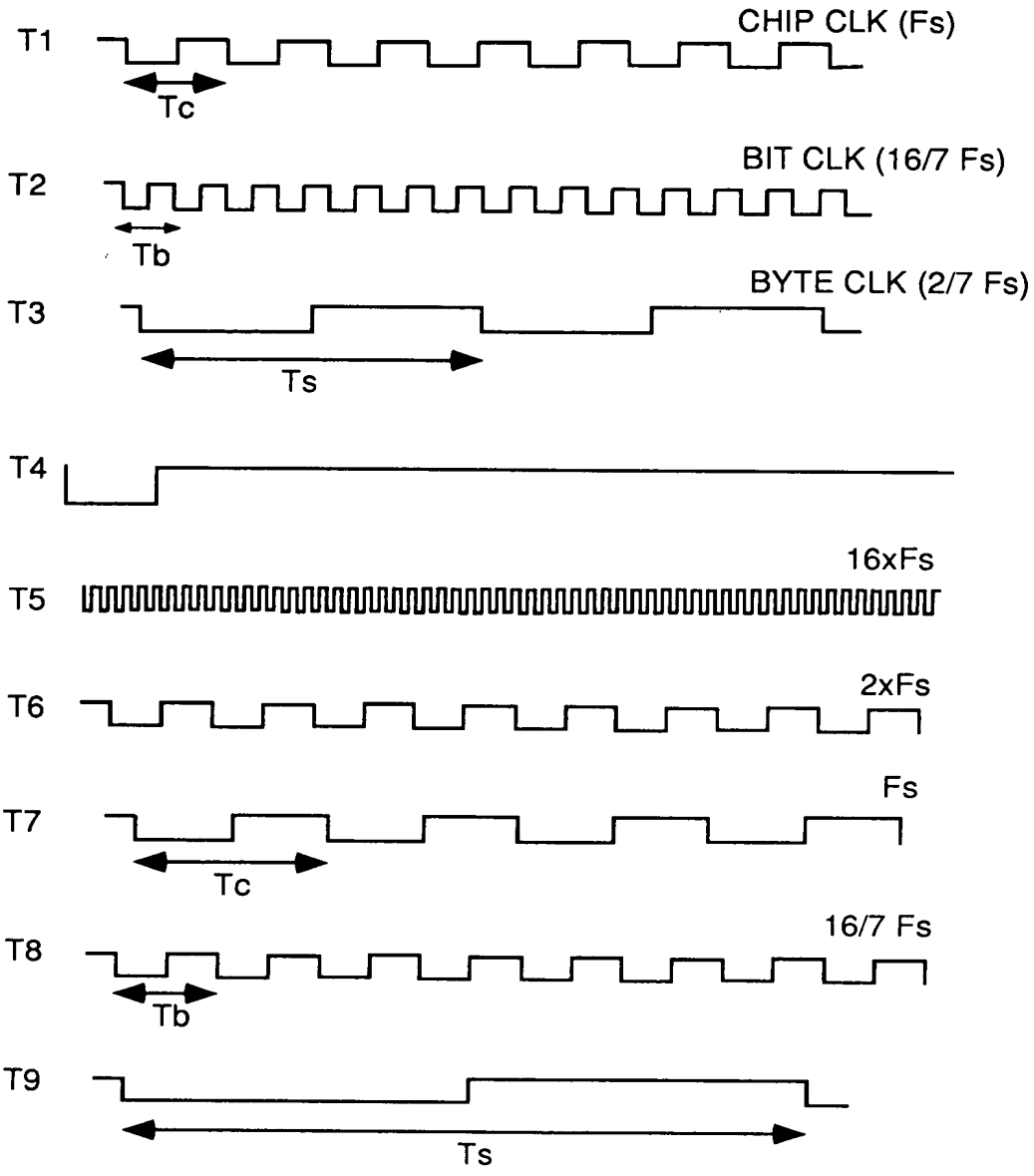

T1
CHIP CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 10

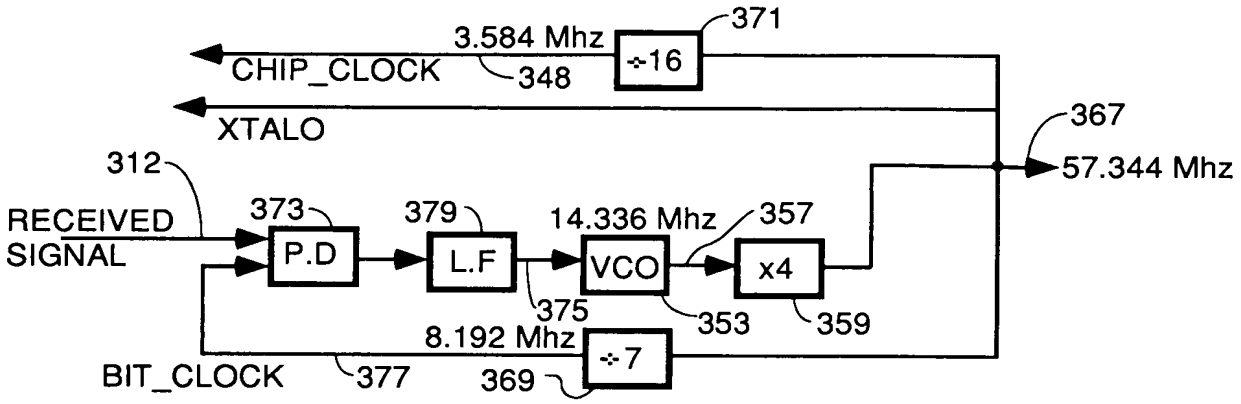


FIG. 11

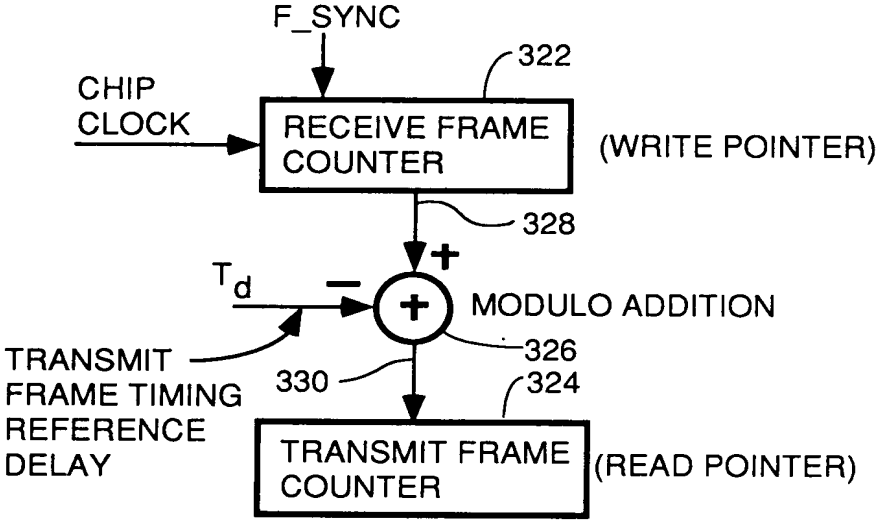


FIG. 12

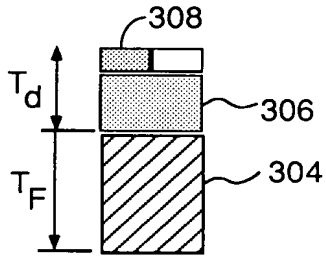


FIG. 13

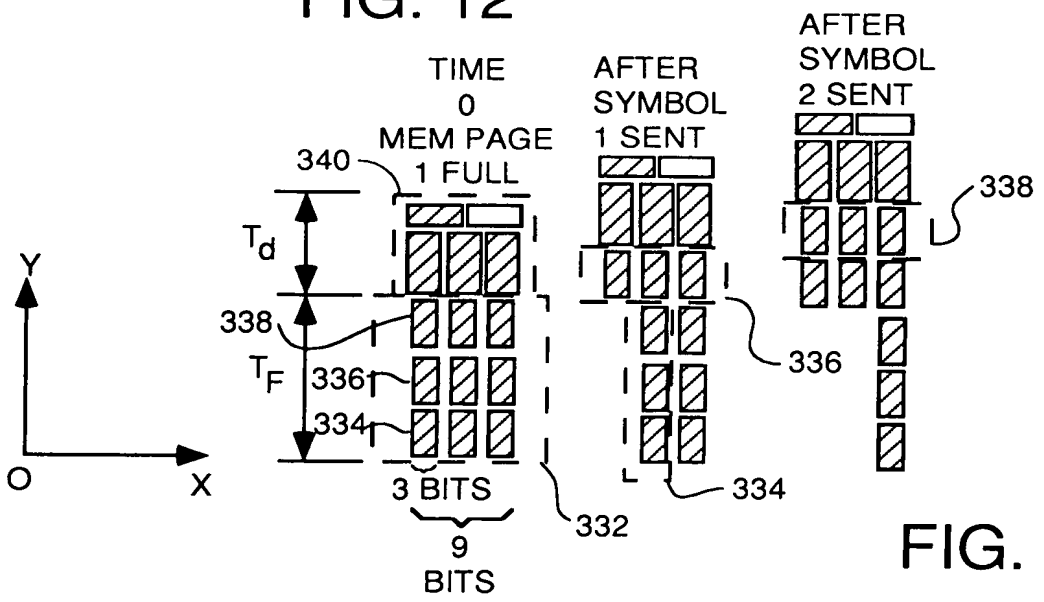


FIG. 14

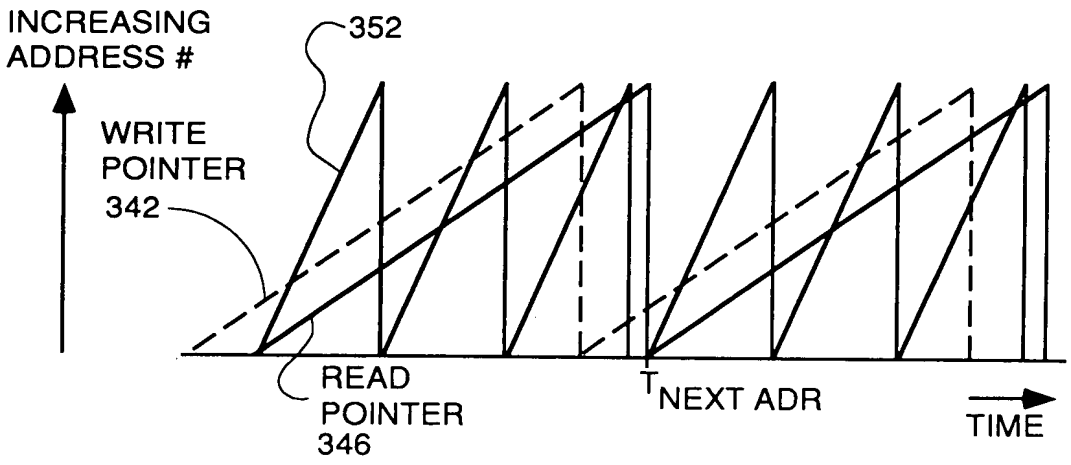

INCREASING
ADDRESS #
352
WRITE
POINTER
342
READ
POINTER
346
T
NEXT ADR
TIME

FIG. 15

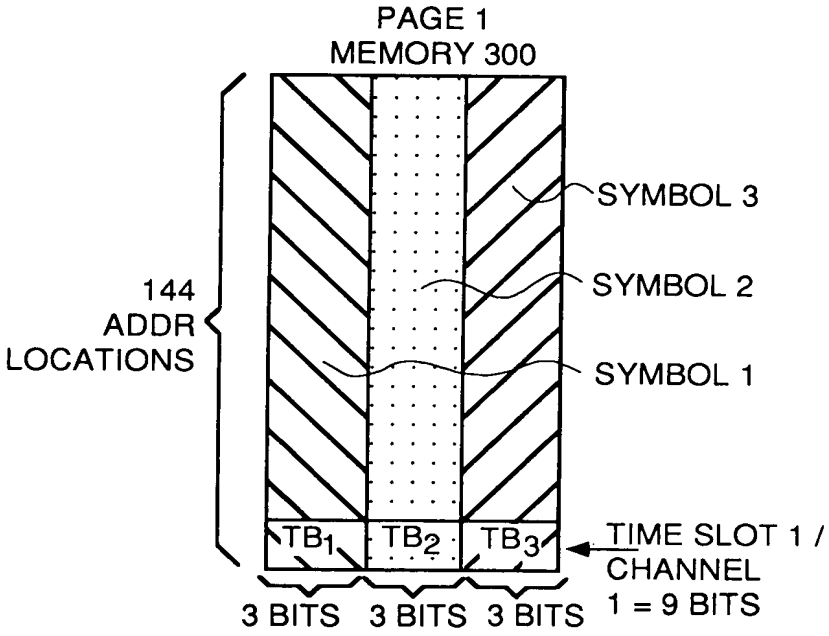
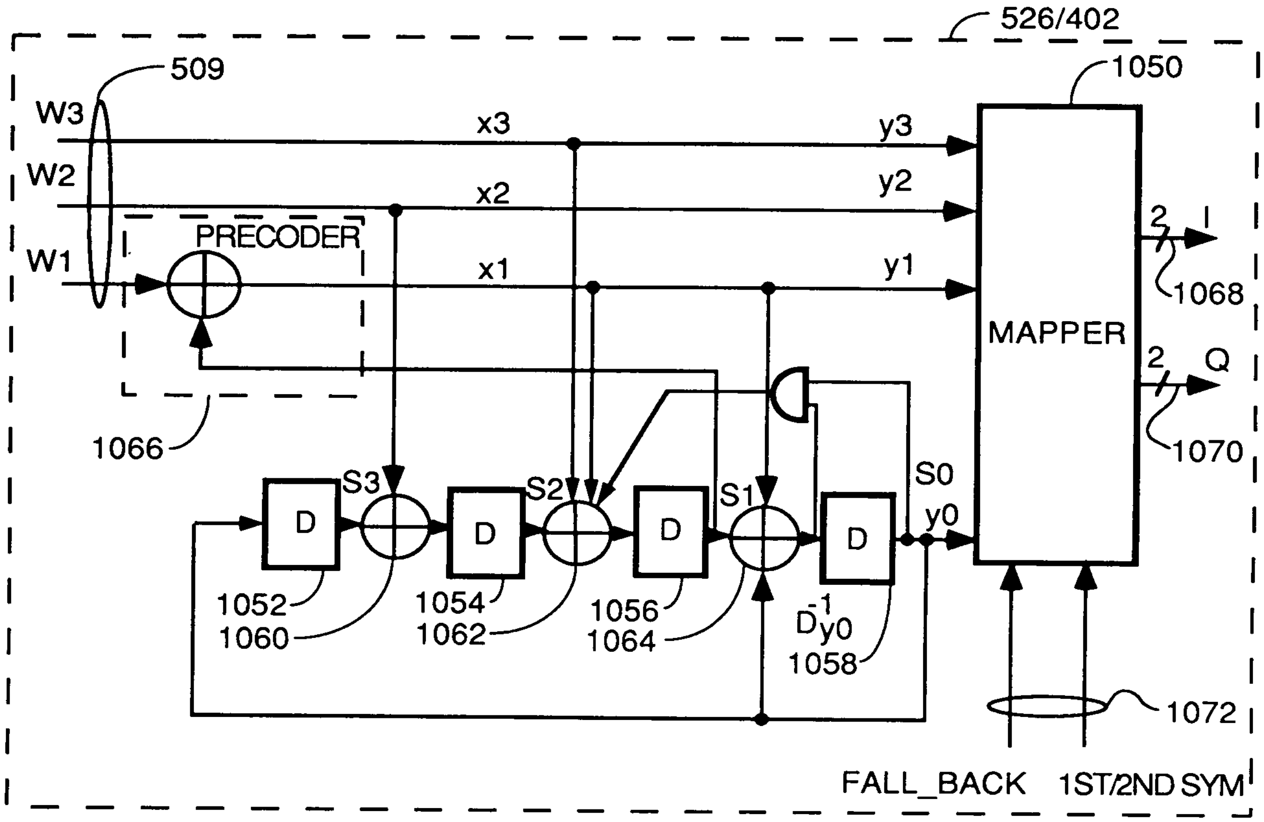

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS 3 BITS 3 BITS

FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

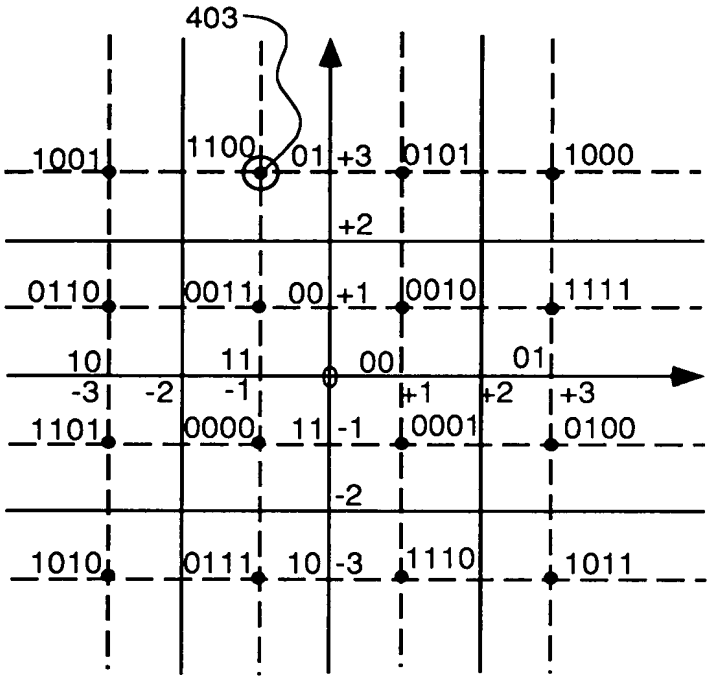


FIG. 18

0000	111	111	
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3*j
1001	101	011	= -3 + 3*j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
403 → 1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

FIG. 19

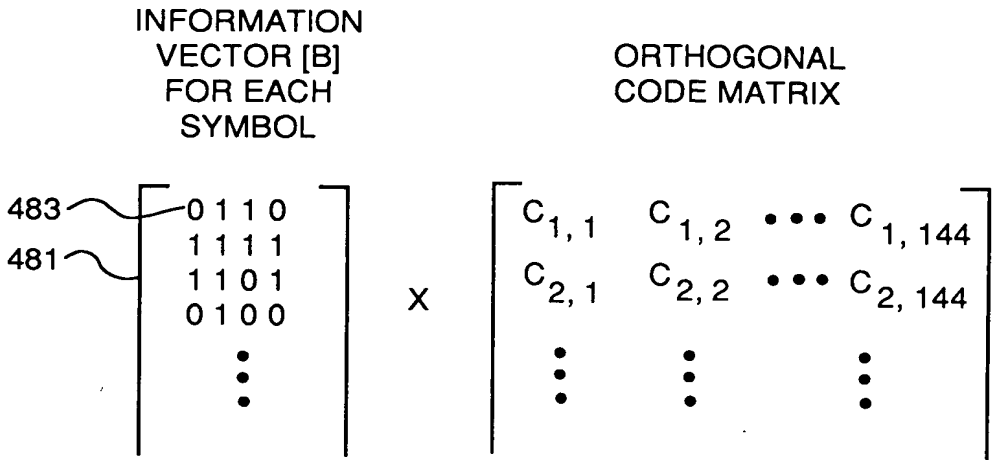


FIG. 20A

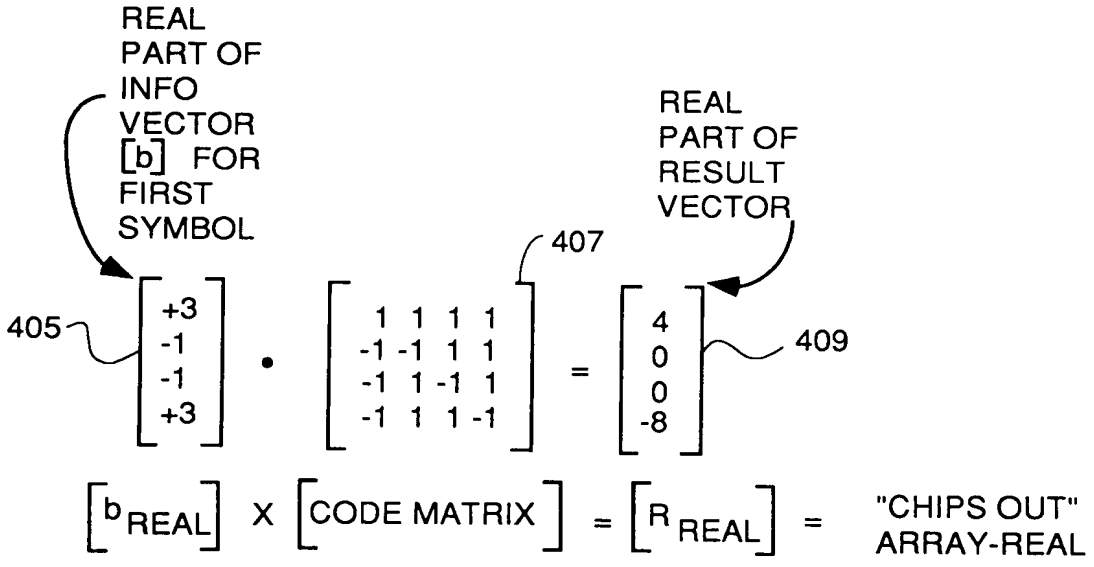


FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

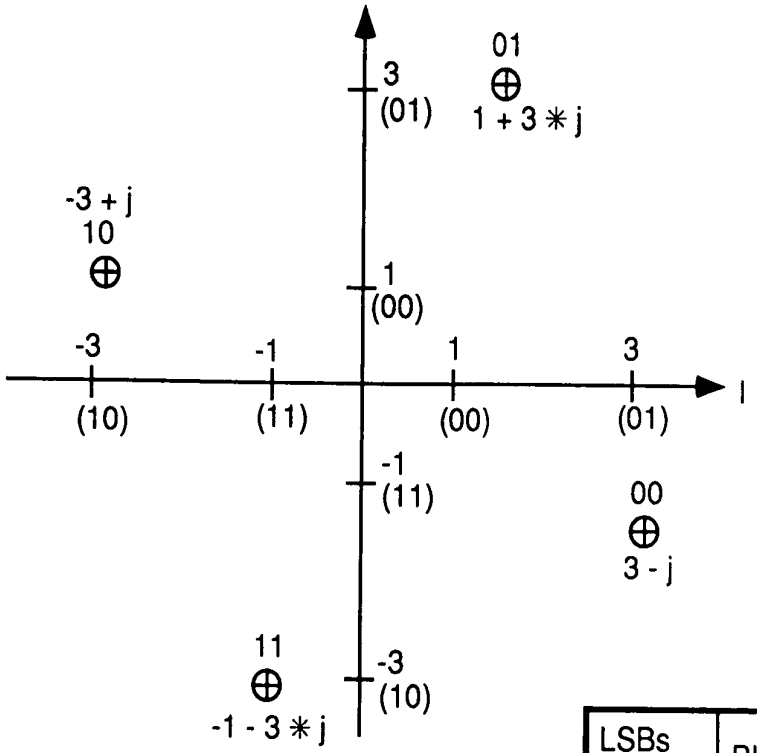


FIG. 21

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

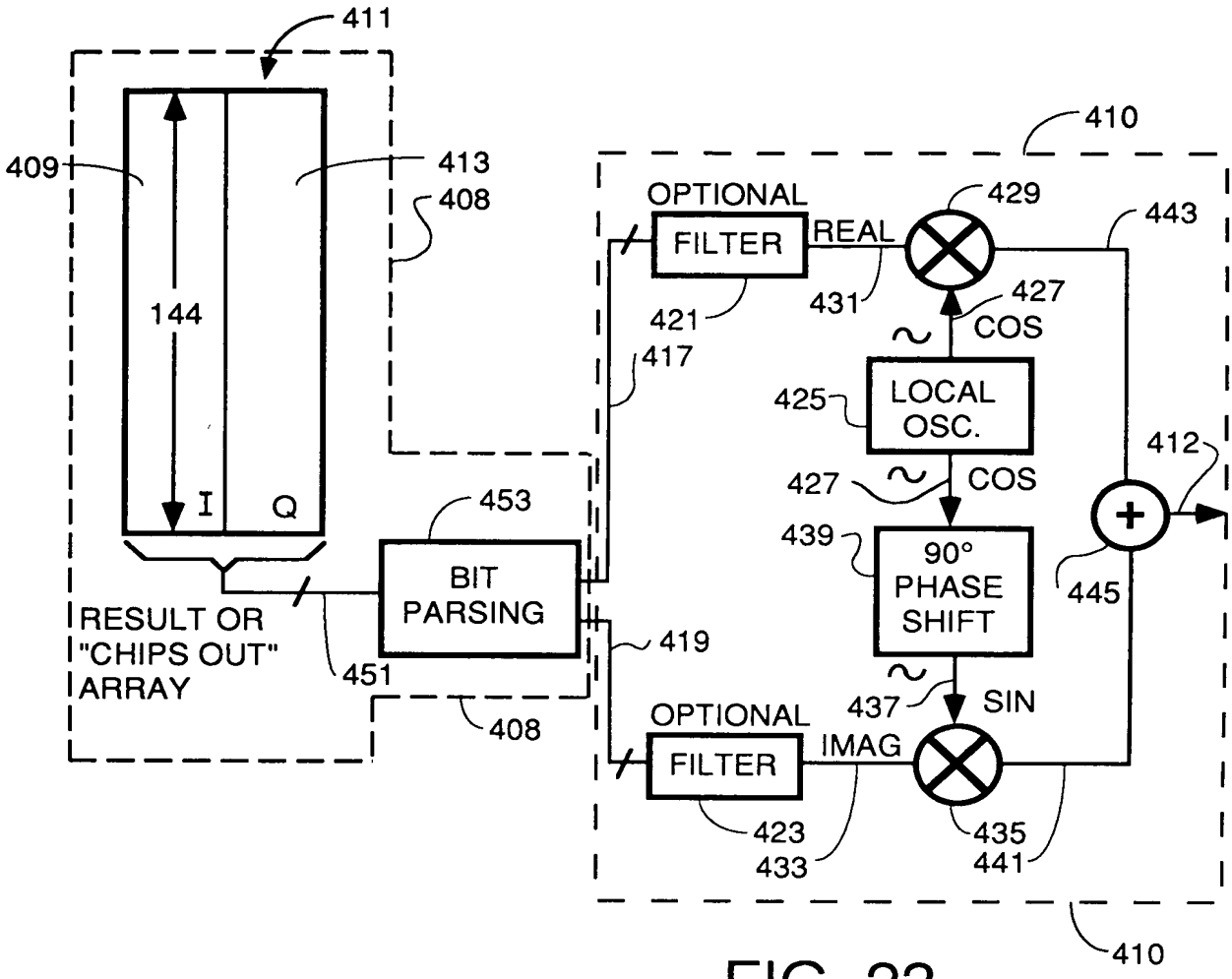

411
409
413
408
144
I
Q
453
BIT
PARSING
RESULT OR
"CHIPS OUT"
ARRAY
451
408
410
OPTIONAL
FILTER
REAL
429
443
421
431
427
COS
417
425
LOCAL
OSC.
412
427
COS
439
90°
PHASE
SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 23

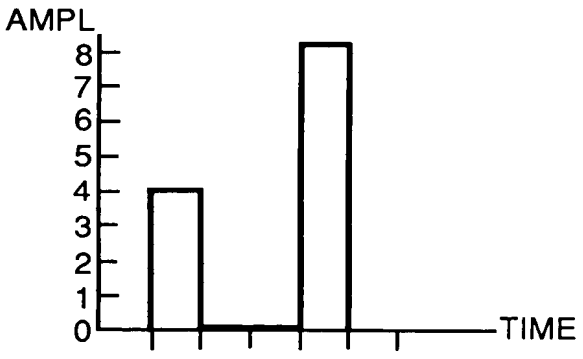

AMPL
8
7
6
5
4
3
2
1
0
TIME

FIG. 24

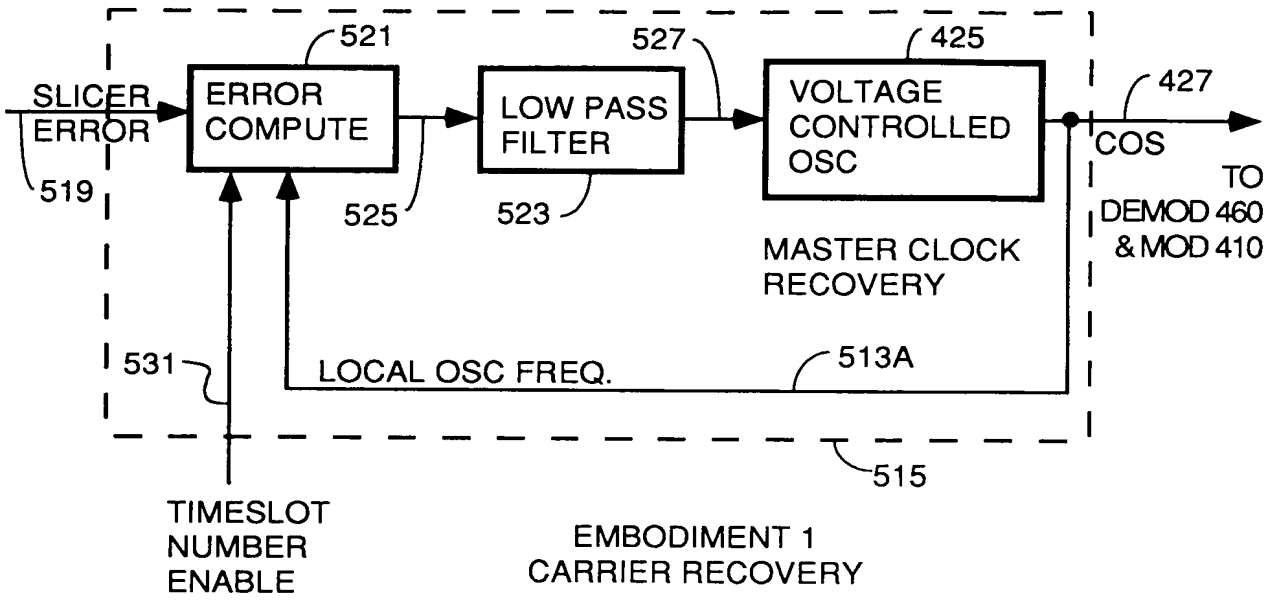

521
527
425
SLICER ERROR
ERROR COMPUTE
LOW PASS FILTER
VOLTAGE CONTROLLED OSC
427
COS
TO DEMOD 460 & MOD 410
519
525
523
MASTER CLOCK RECOVERY
531
LOCAL OSC FREQ.
513A
515
TIMESLOT NUMBER ENABLE
EMBODIMENT 1 CARRIER RECOVERY

FIG. 25

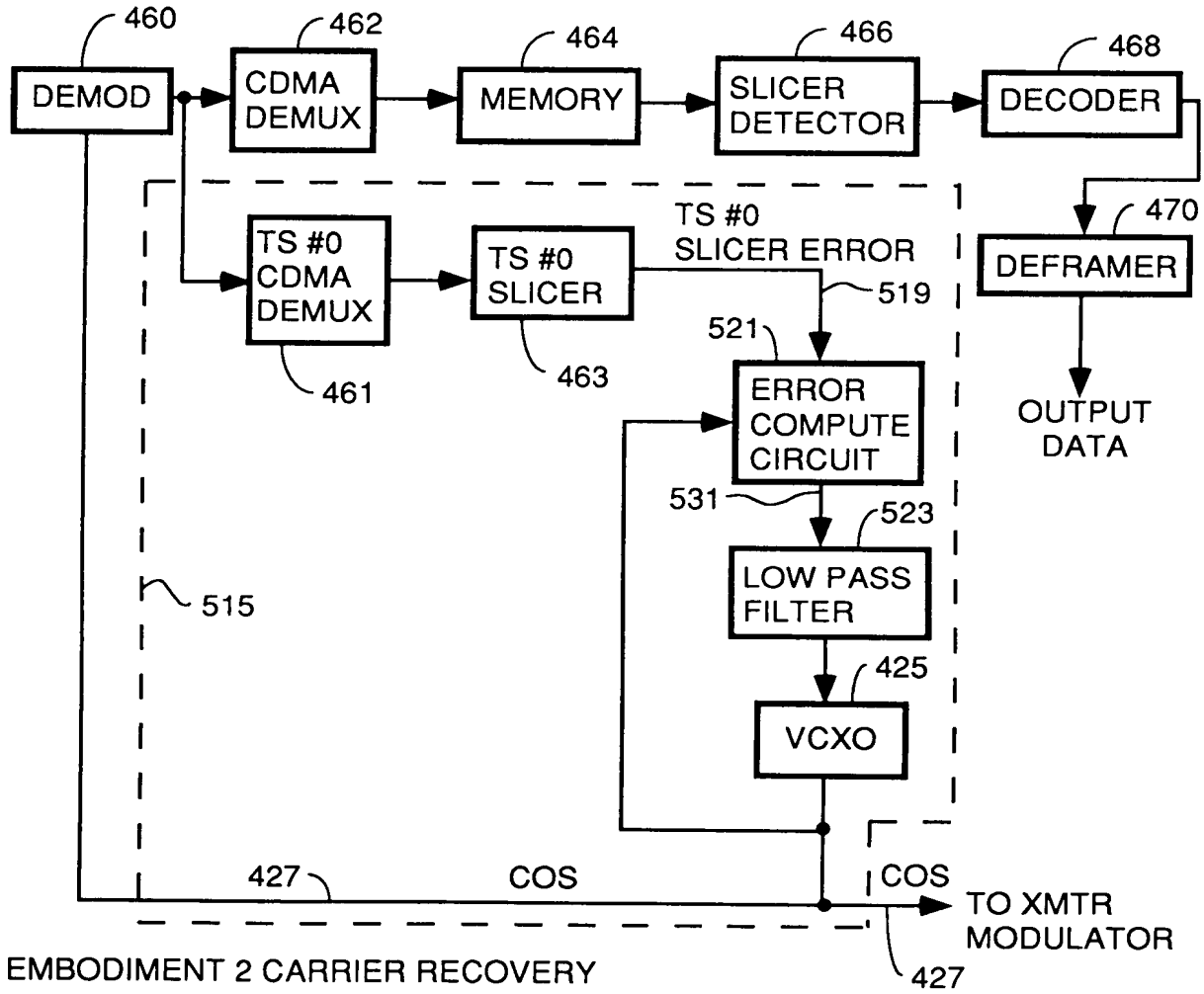

460
462
464
466
468
DEMOD
CDMA DEMUX
MEMORY
SLICER DETECTOR
DECODER
TS #0 SLICER ERROR
470
TS #0 CDMA DEMUX
TS #0 SLICER
DEFRAMER
519
521
461
463
ERROR COMPUTE CIRCUIT
OUTPUT DATA
531
523
LOW PASS FILTER
515
425
VCXO
427
COS
COS
TO XMTR MODULATOR
EMBODIMENT 2 CARRIER RECOVERY
427

FIG. 26

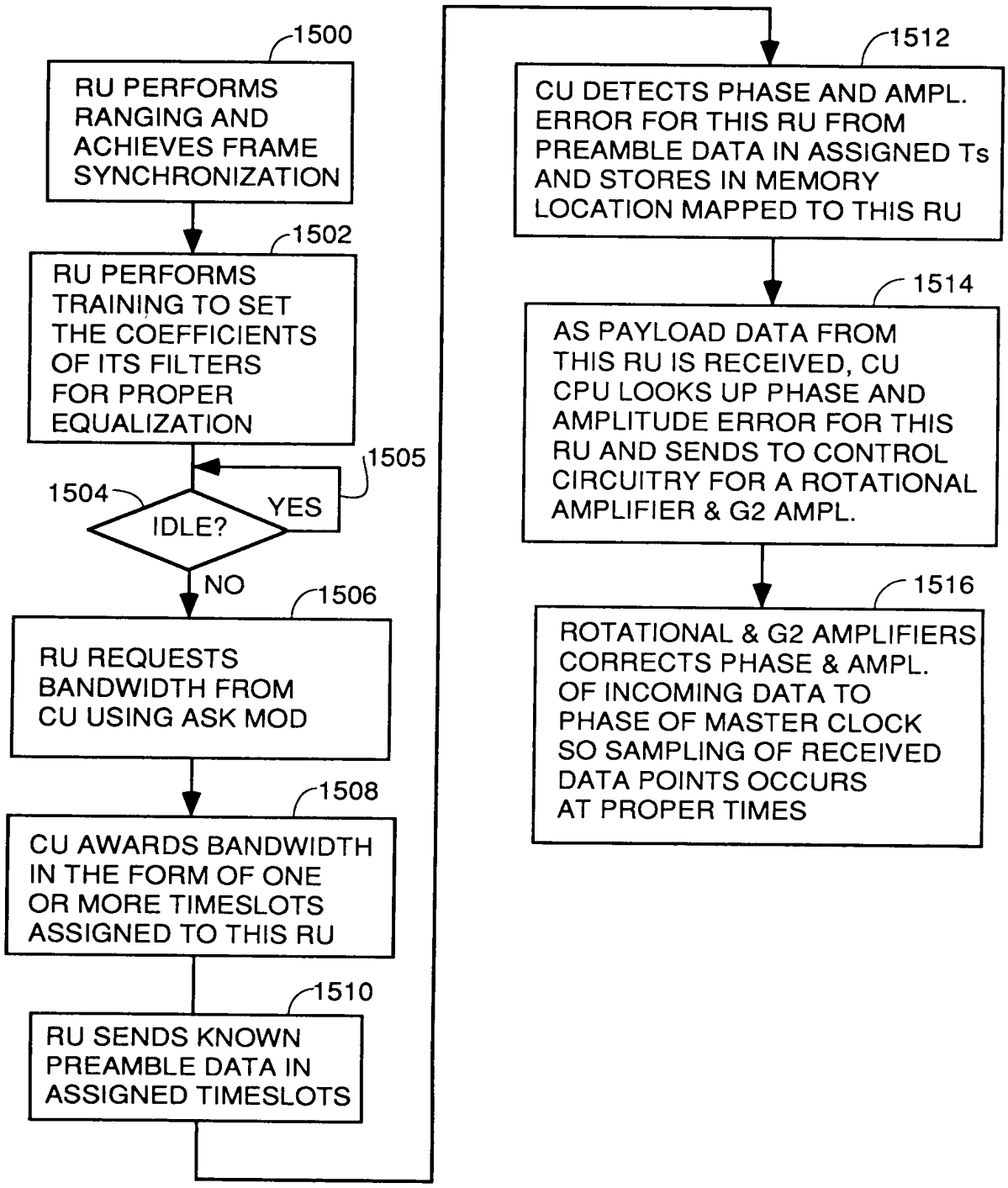
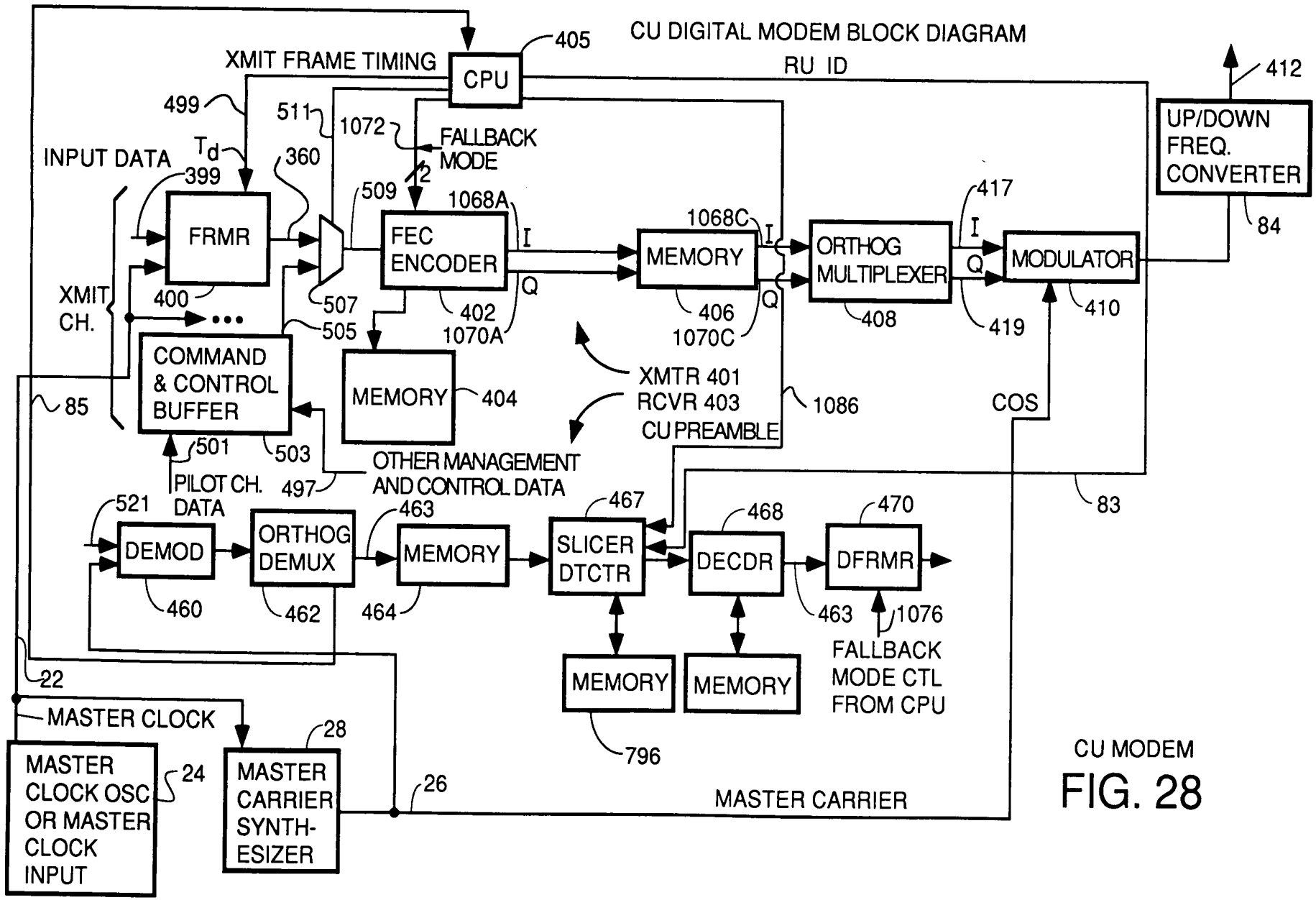


FIG. 27



CU MODEM

FIG. 28

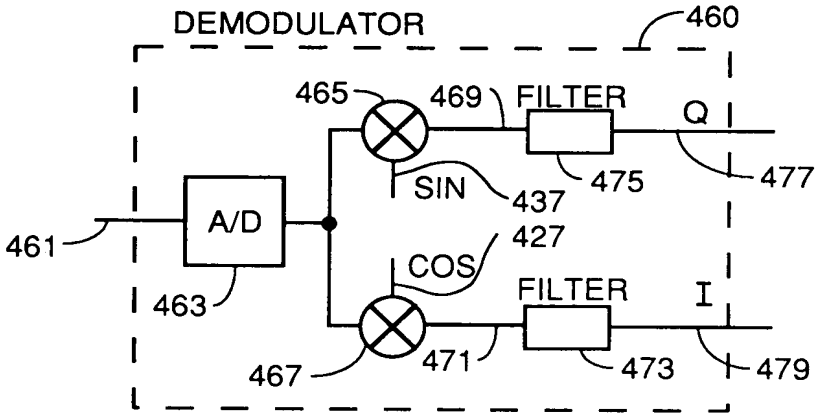


FIG. 29

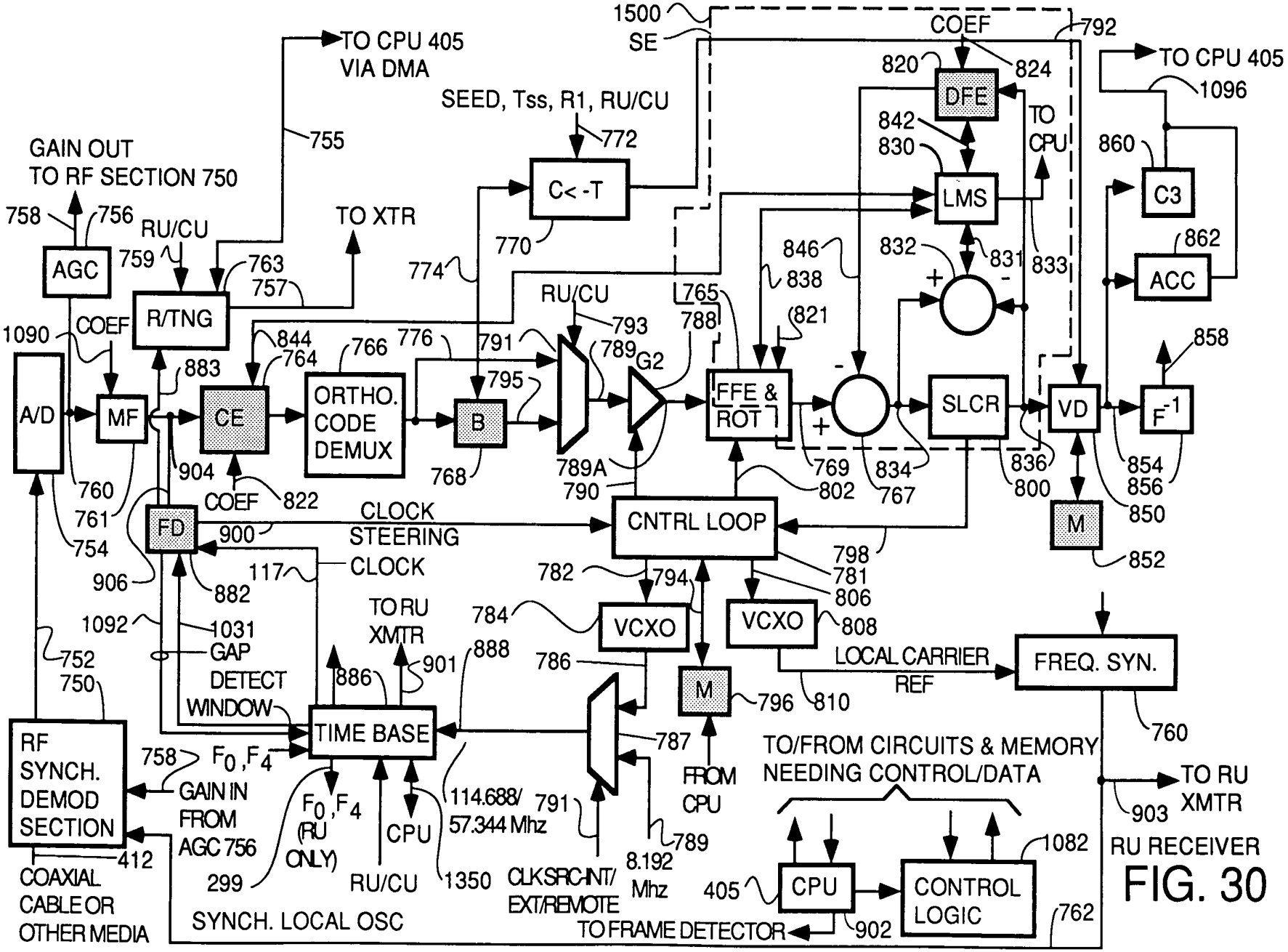
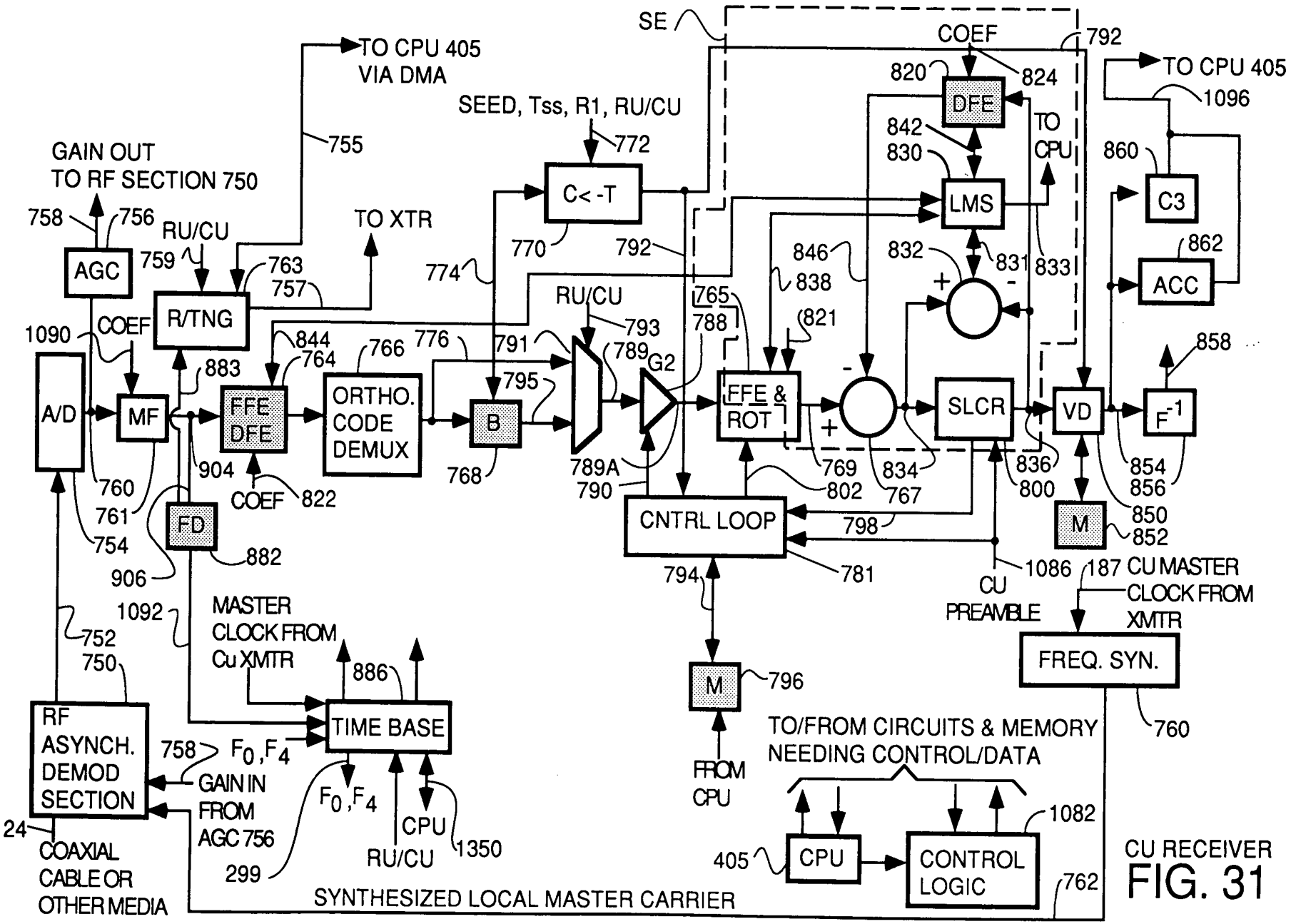
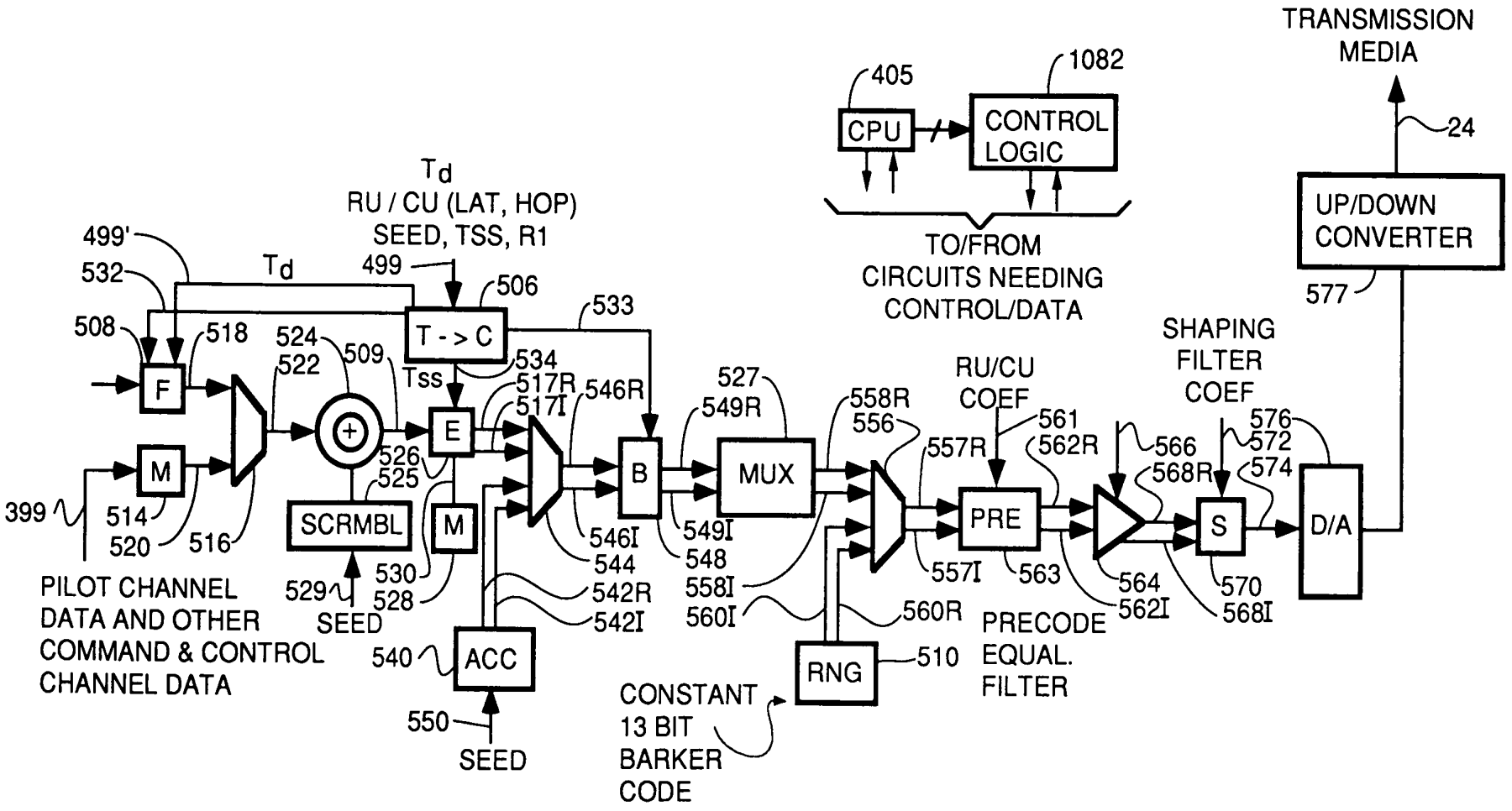

1500
SE
COEF
792
TO CPU 405
VIA DMA
SEED, Tss, R1, RU/CU
772
820
824
DFE
TO CPU 405
1096
842
830
TO CPU
860
GAIN OUT
TO RF SECTION 750
755
C<-T
LMS
C3
758
756
RU/CU
TO XTR
770
846
832
831
833
862
759
763
757
774
838
AGC
ACC
R/TNG
RU/CU
765
788
793
821
858
1090
COEF
844
766
776
791
789
G2
764
883
795
A/D
MF
CE
ORTHO. CODE DEMUX
B
FFE & ROT
SLCR
VD
F-1
904
768
789A
769
834
836
854
760
COEF
822
790
802
767
800
856
761
CLOCK
STEERING
CNTRL LOOP
M
850
FD
900
754
798
906
117
CLOCK
781
852
782
794
882
806
TO RU
XMTR
784
VCXO
VCXO
808
1092
1031
888
752
GAP
786
LOCAL CARRIER
FREQ. SYN.
901
DETECT
886
M
796
810
750
WINDOW
760
RF
SYNCH.
DEMOD
SECTION
TIME BASE
787
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
758
F0, F4
FROM
CPU
TO RU
XMTR
GAIN IN
FROM
AGC 756
F0, F4
(RU
ONLY)
CPU
114.688/
57.344 Mhz
791
789
1082
903
RU RECEIVER
412
8.192
Mhz
405
CPU
CONTROL
LOGIC
COAXIAL
CABLE OR
OTHER MEDIA
299
RU/CU
1350
CLKSRC-INT/
EXT/REMOTE
902
762
SYNCH. LOCAL OSC
TO FRAME DETECTOR

FIG. 30



CU RECEIVER

FIG. 31



CU TRANSMITTER

FIG. 32

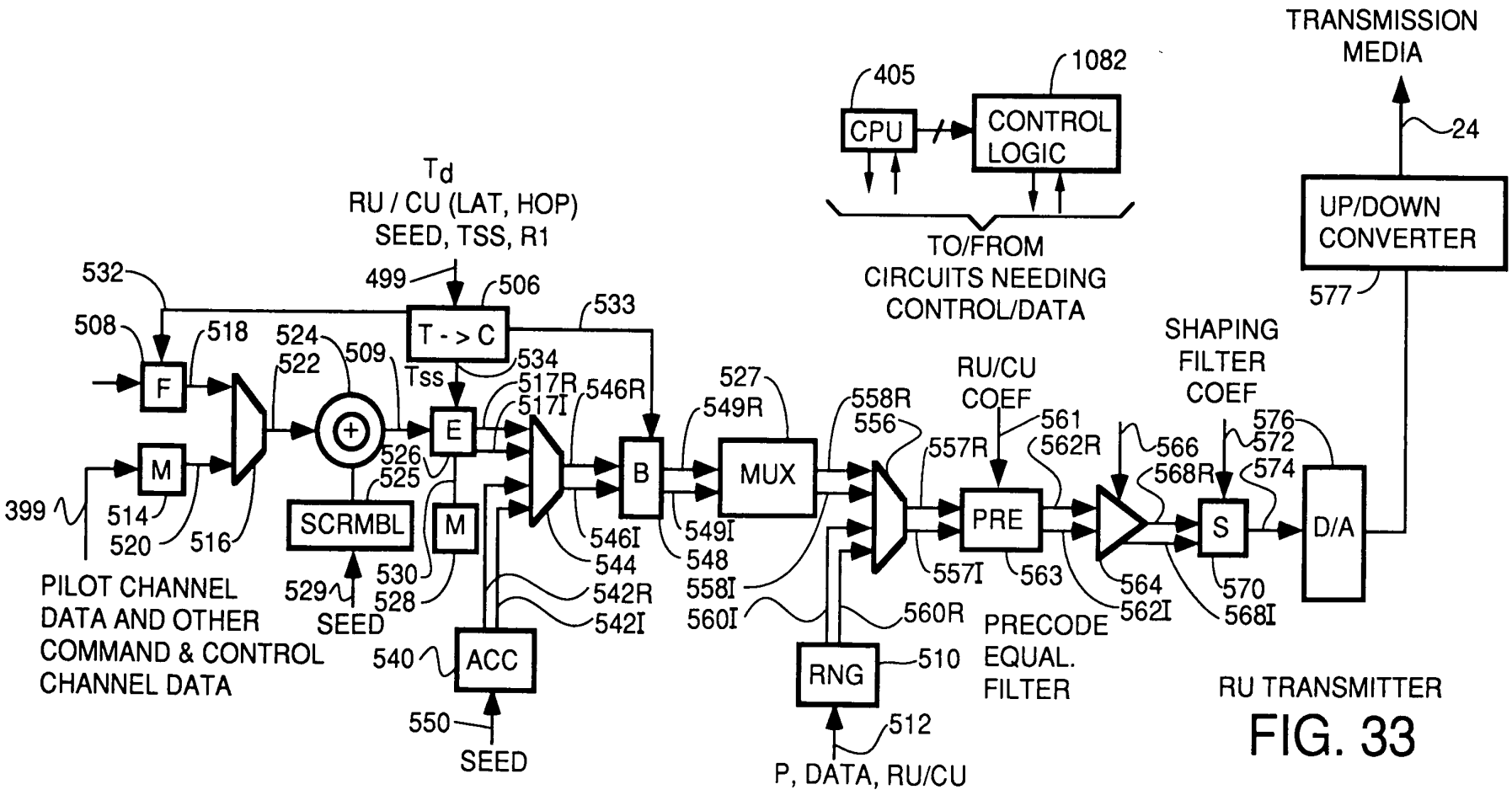


FIG. 33

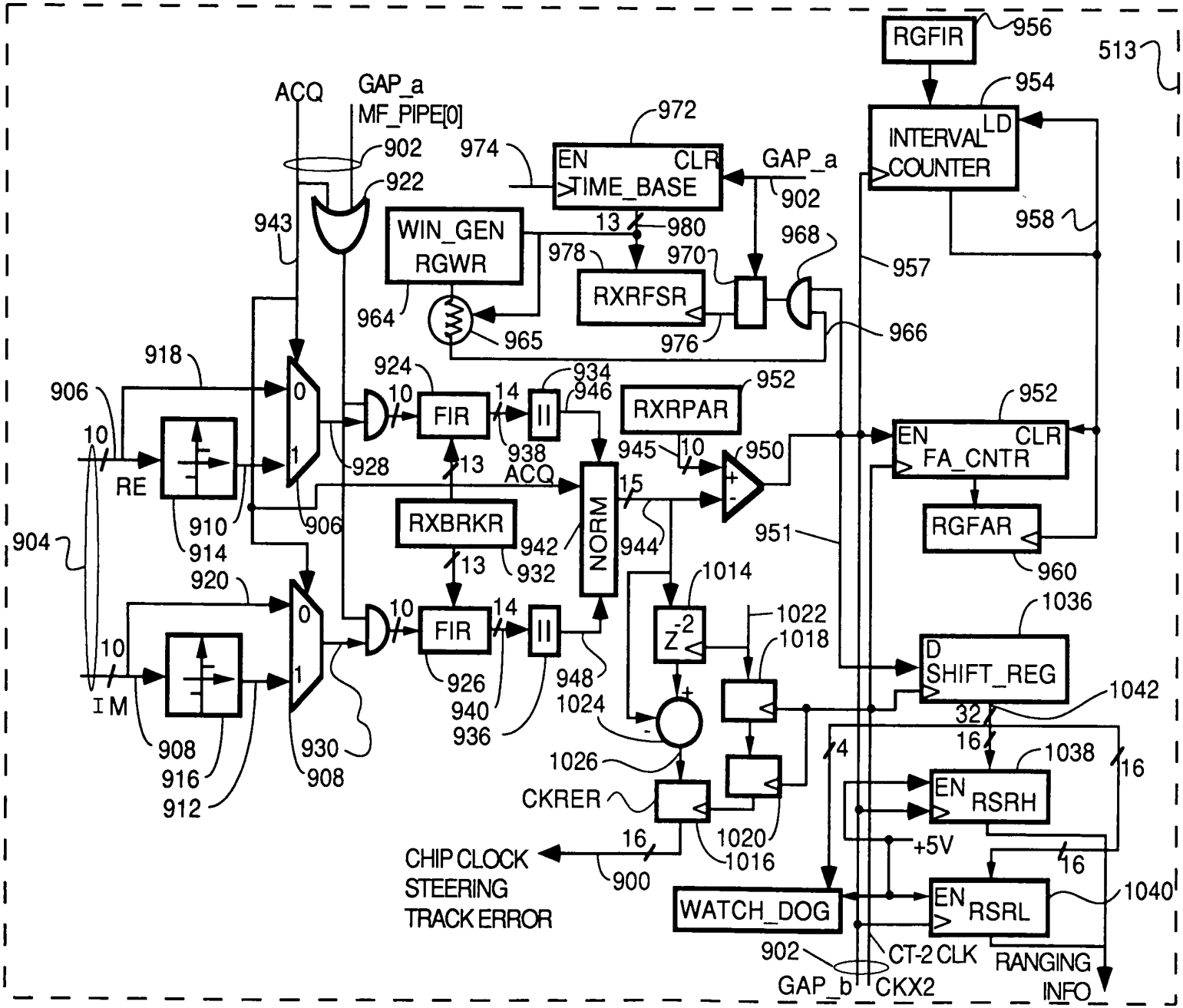


FIG. 34

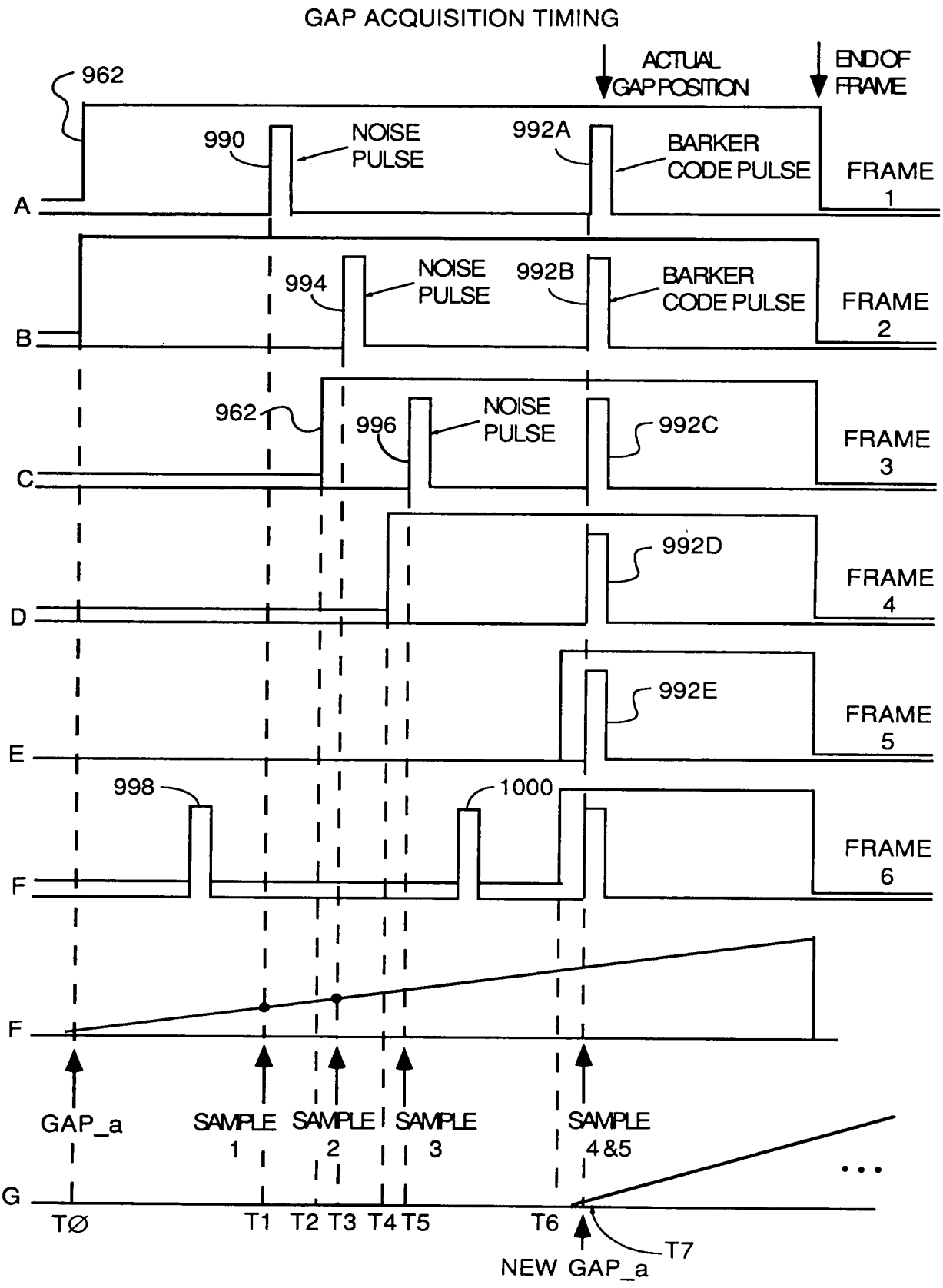

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1
T2
T3
T4
T5
T6
T7
NEW GAP_a

FIG. 35

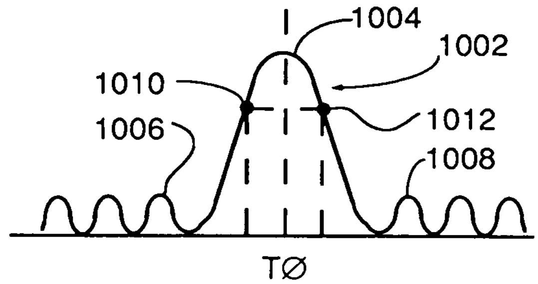


FIG. 36

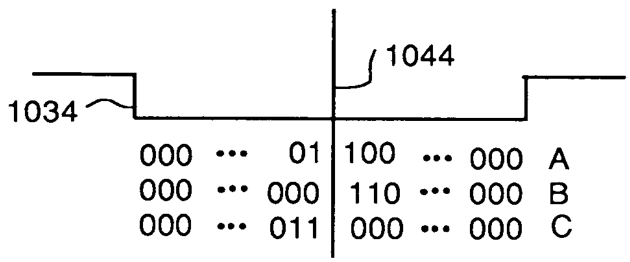


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

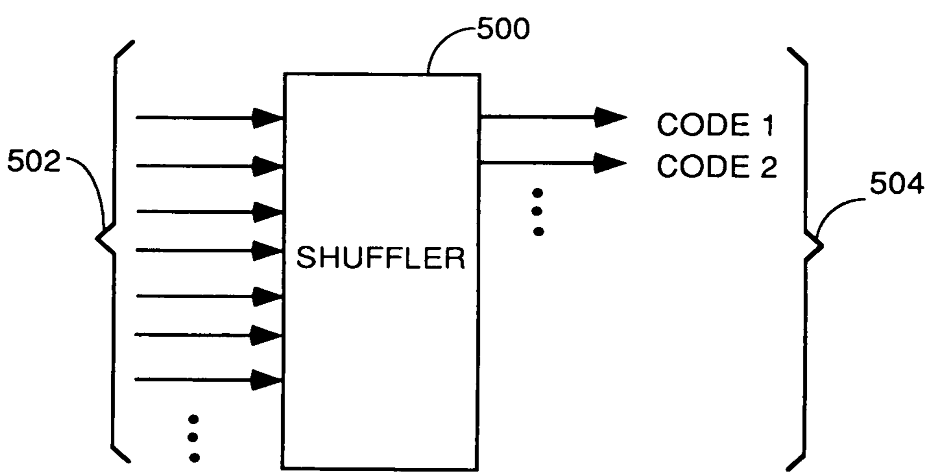


FIG. 38

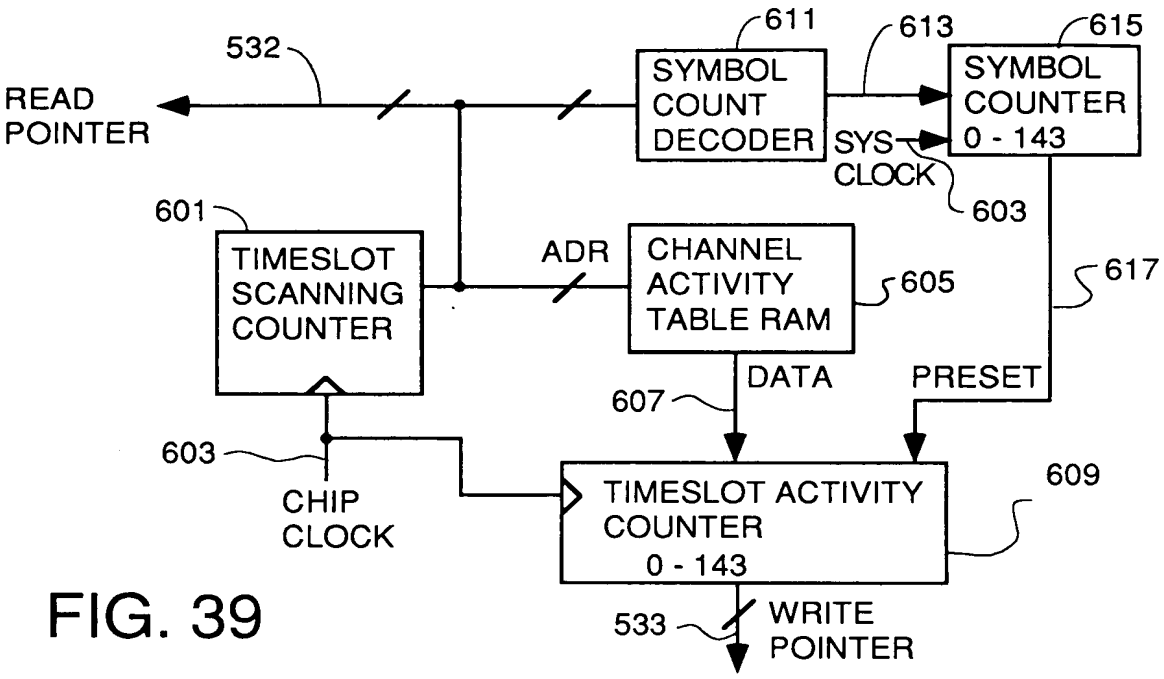


FIG. 39

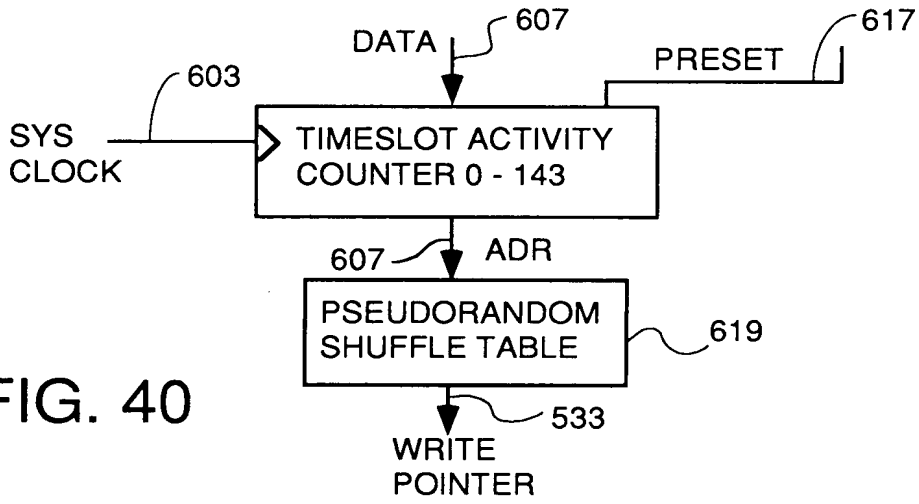


FIG. 40

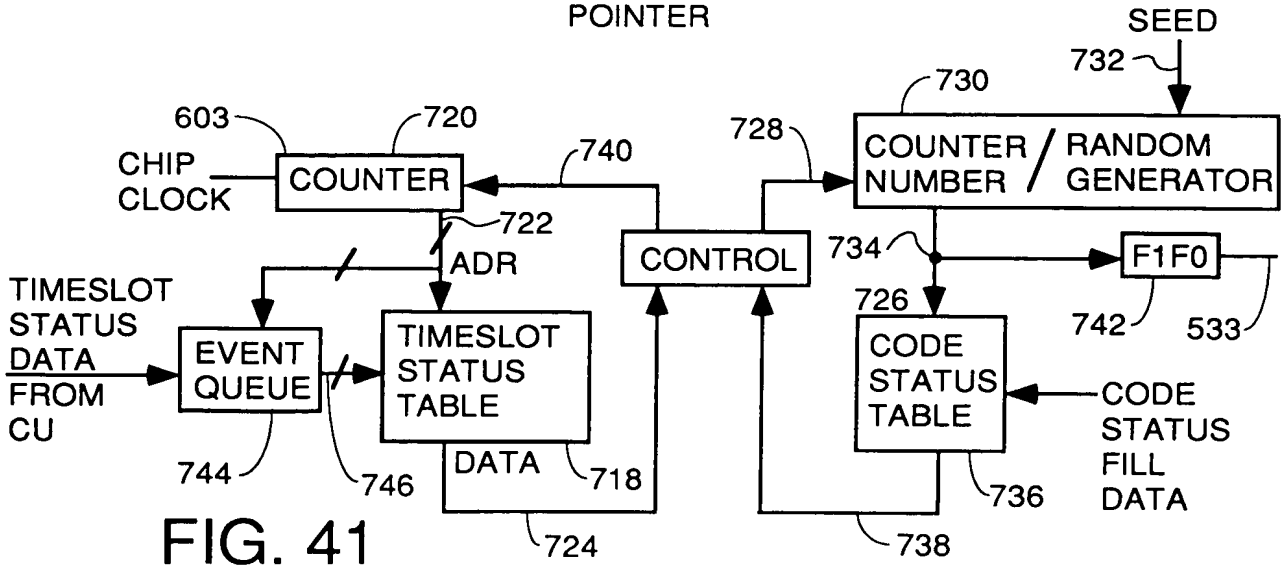


FIG. 41

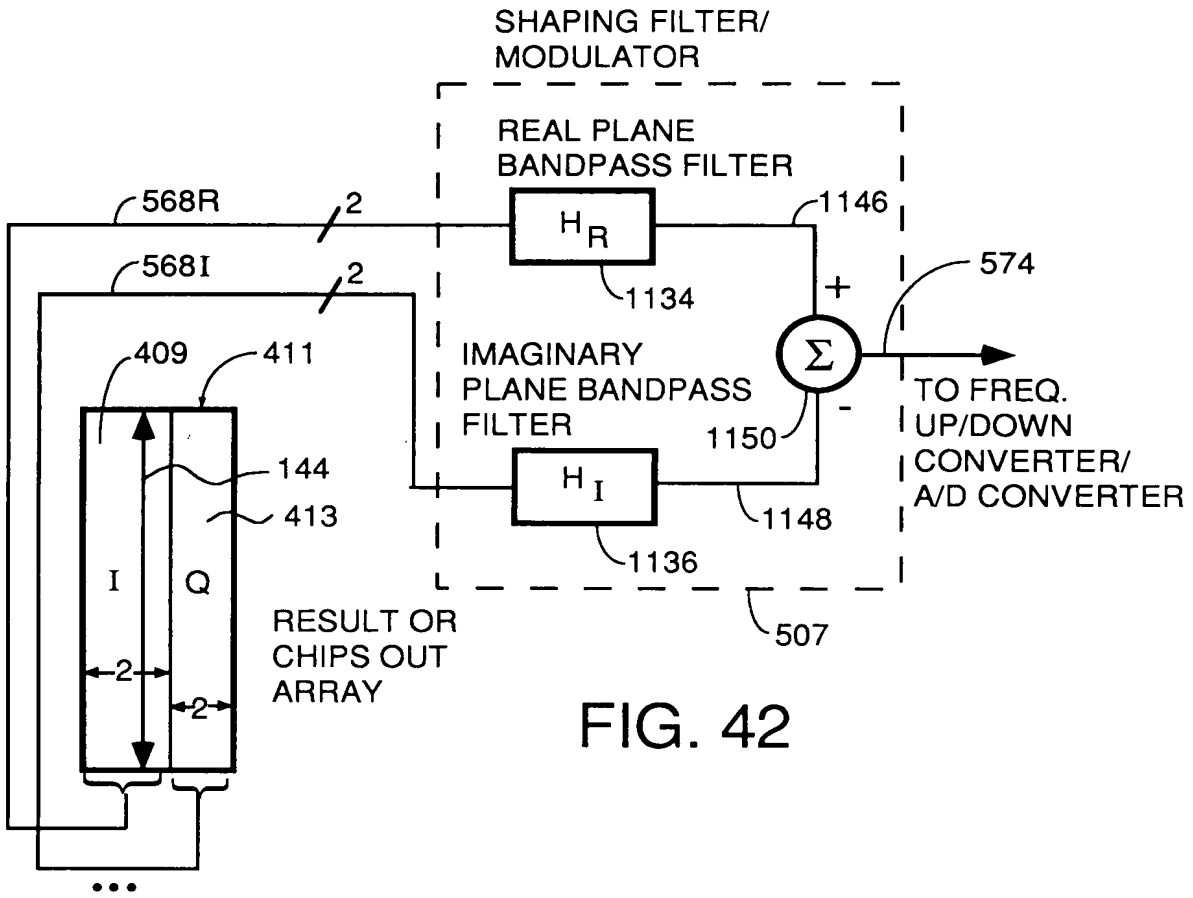


FIG. 42

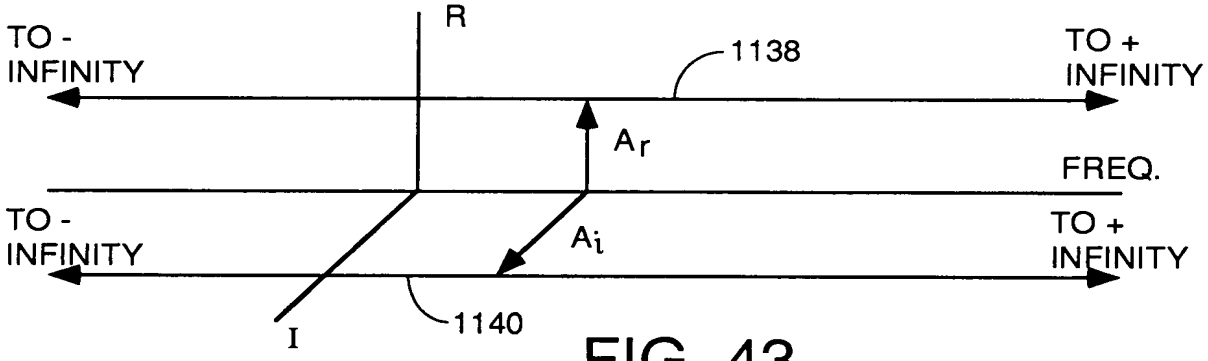


FIG. 43

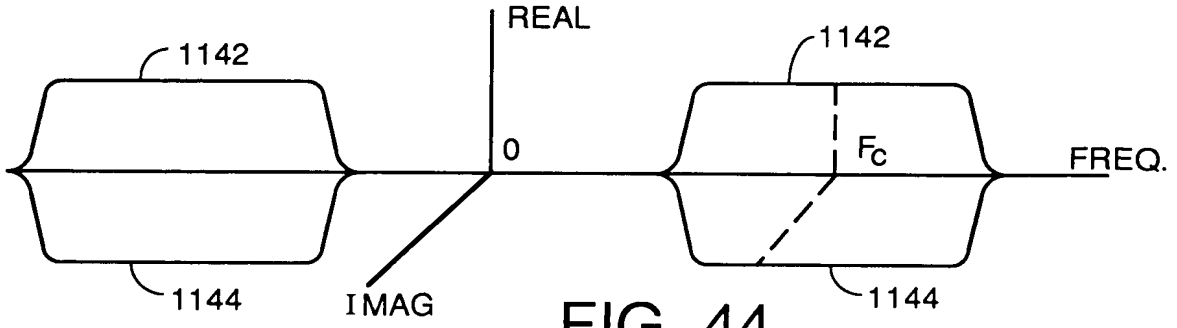
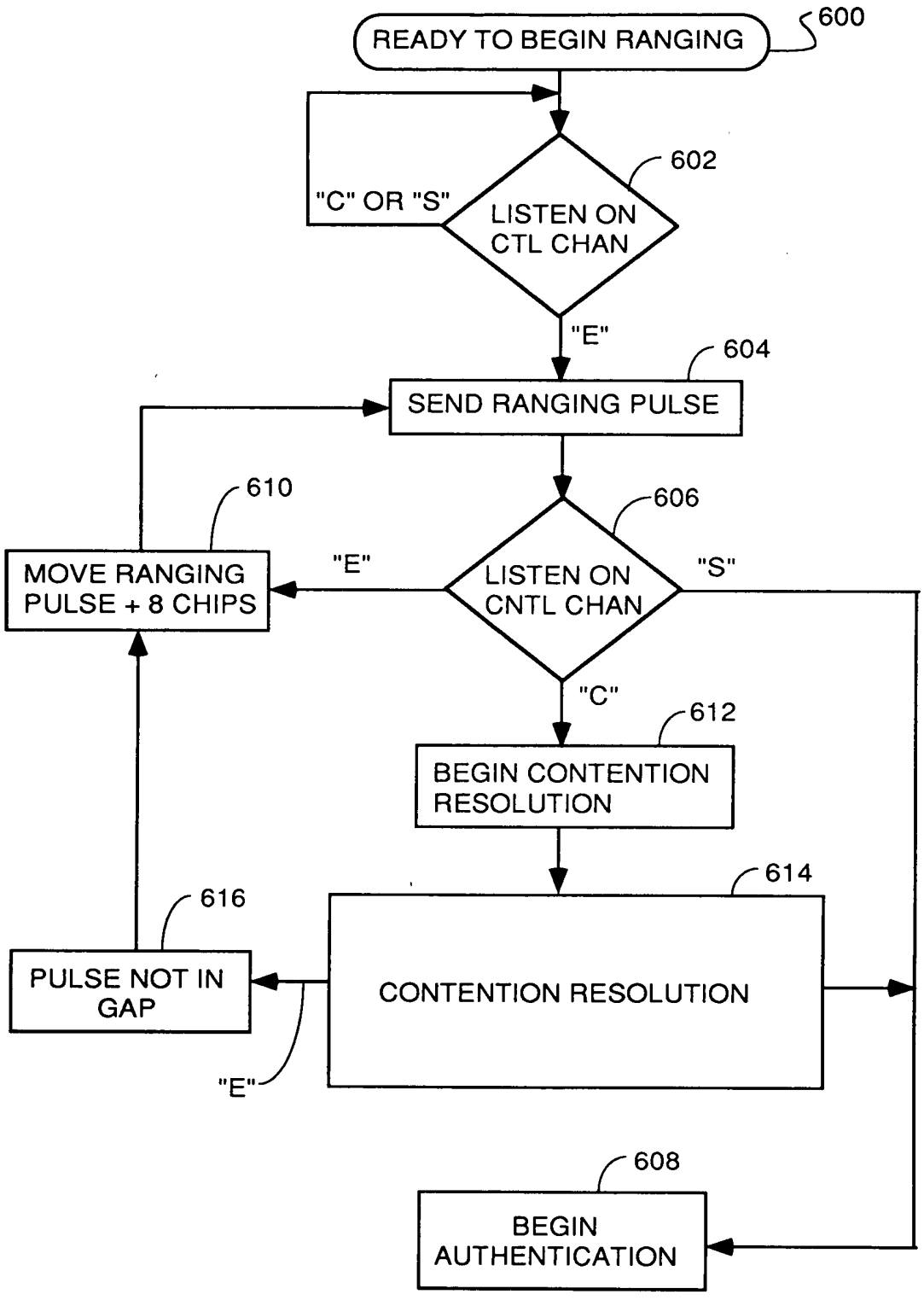
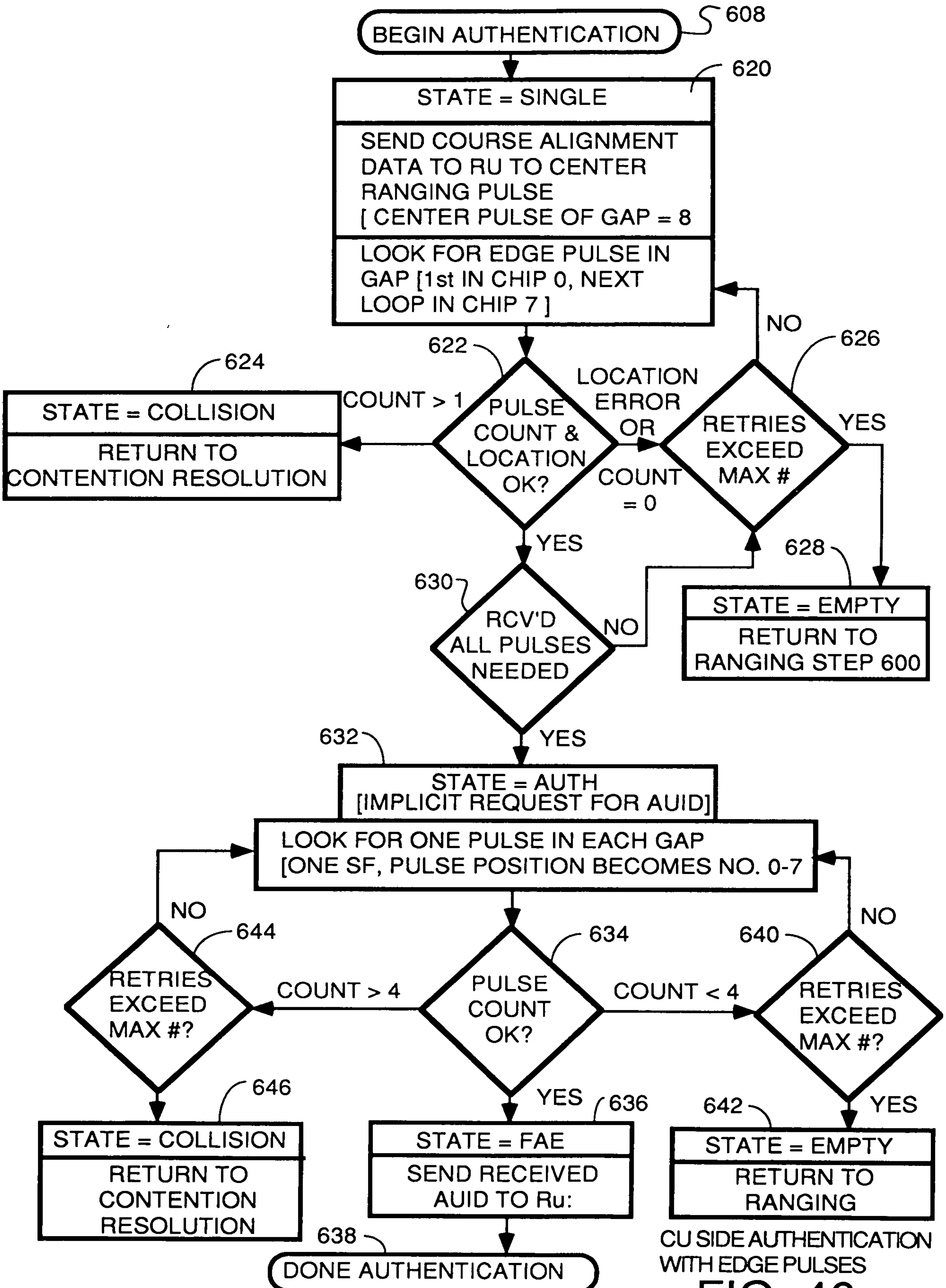


FIG. 44



RU RANGING

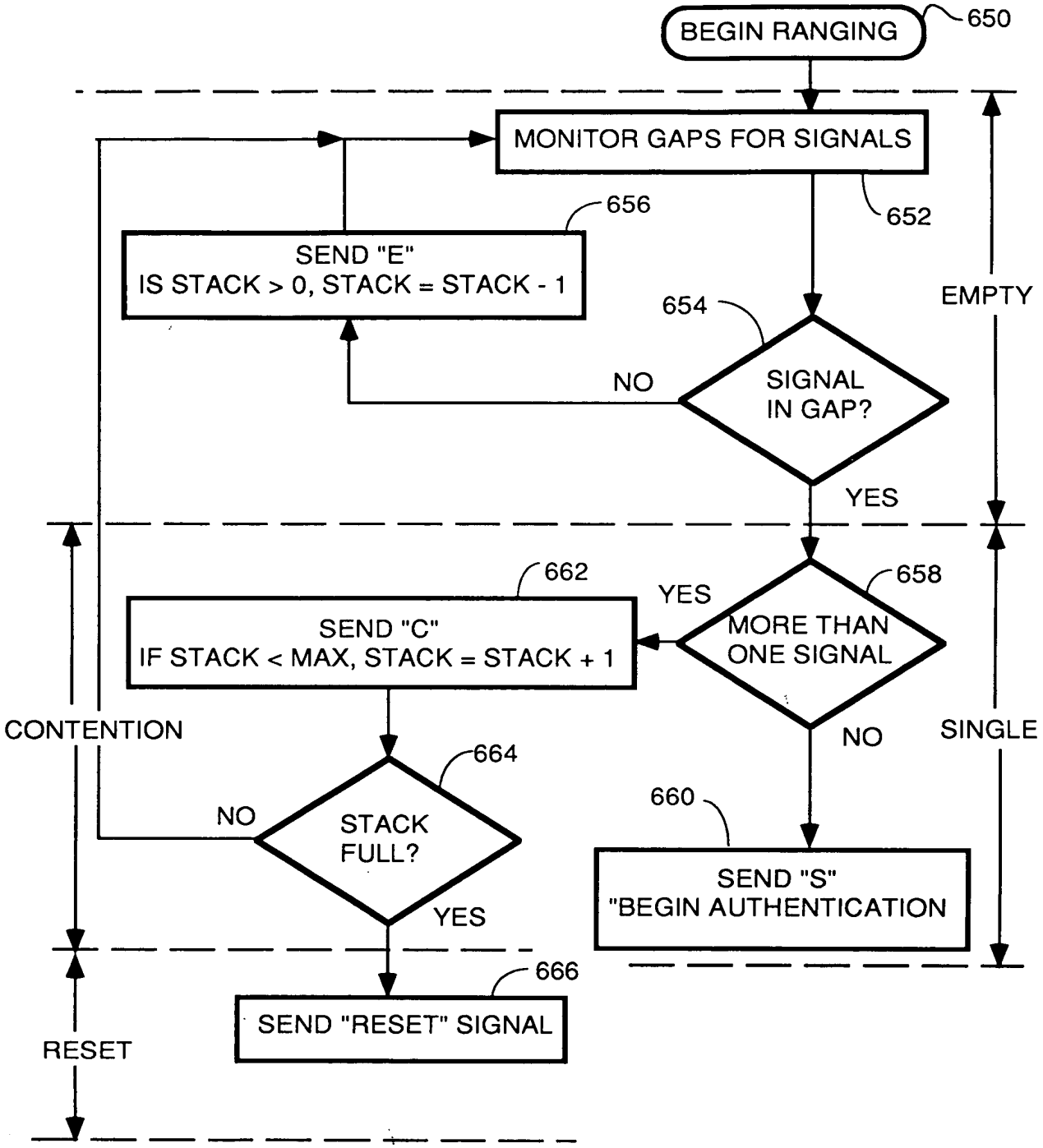
FIG. 45


BEGIN AUTHENTICATION
608
STATE = SINGLE
620
SEND COURSE ALIGNMENT DATA TO RU TO CENTER RANGING PULSE [CENTER PULSE OF GAP = 8
LOOK FOR EDGE PULSE IN GAP [1st IN CHIP 0, NEXT LOOP IN CHIP 7]
622
PULSE COUNT & LOCATION OK?
COUNT > 1
624
STATE = COLLISION
RETURN TO CONTENTION RESOLUTION
LOCATION ERROR OR COUNT = 0
626
RETRIES EXCEED MAX #
NO
YES
628
STATE = EMPTY
RETURN TO RANGING STEP 600
YES
630
RCV'D ALL PULSES NEEDED
NO
YES
632
STATE = AUTH [IMPLICIT REQUEST FOR AUID]
LOOK FOR ONE PULSE IN EACH GAP [ONE SF, PULSE POSITION BECOMES NO. 0-7
634
PULSE COUNT OK?
COUNT > 4
COUNT < 4
644
RETRIES EXCEED MAX #?
NO
640
RETRIES EXCEED MAX #?
NO
YES
636
646
STATE = COLLISION
RETURN TO CONTENTION RESOLUTION
STATE = FAE
SEND RECEIVED AUID TO Ru:
642
STATE = EMPTY
RETURN TO RANGING
YES
638
DONE AUTHENTICATION

CU SIDE AUTHENTICATION WITH EDGE PULSES

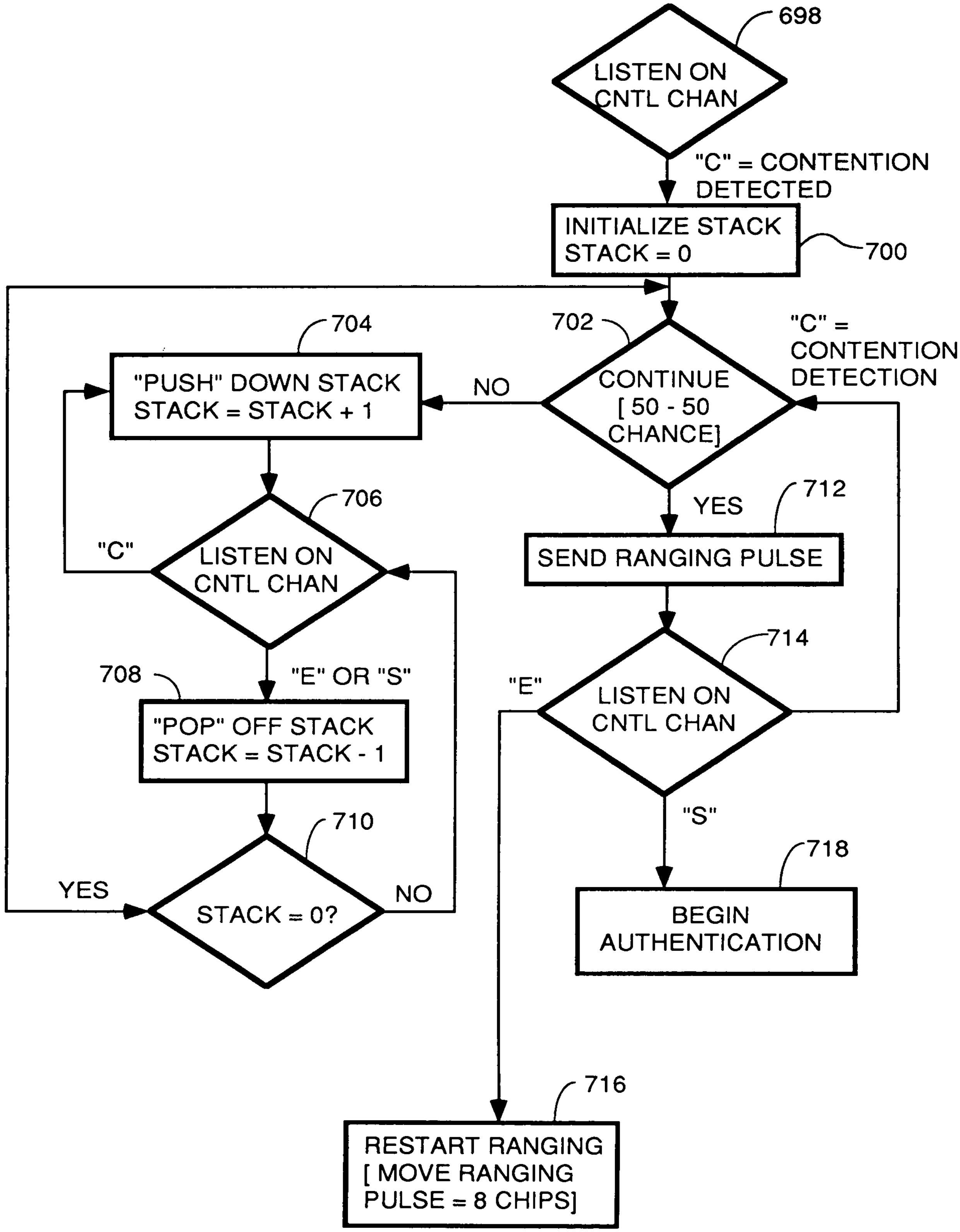
FIG. 46

10232427 . 041201



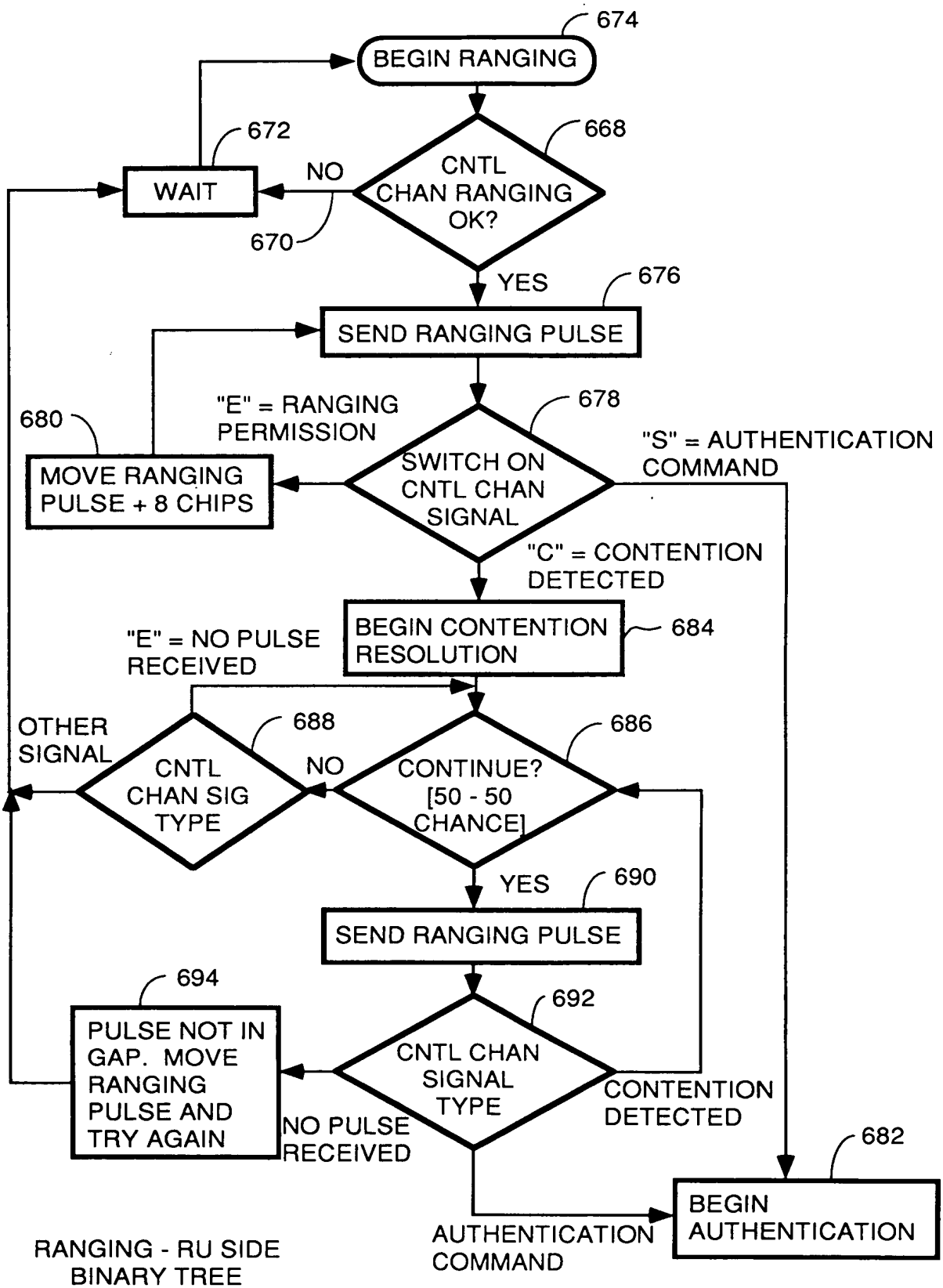
CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48



RANGING - RU SIDE BINARY TREE ALGORITHM

FIG. 49

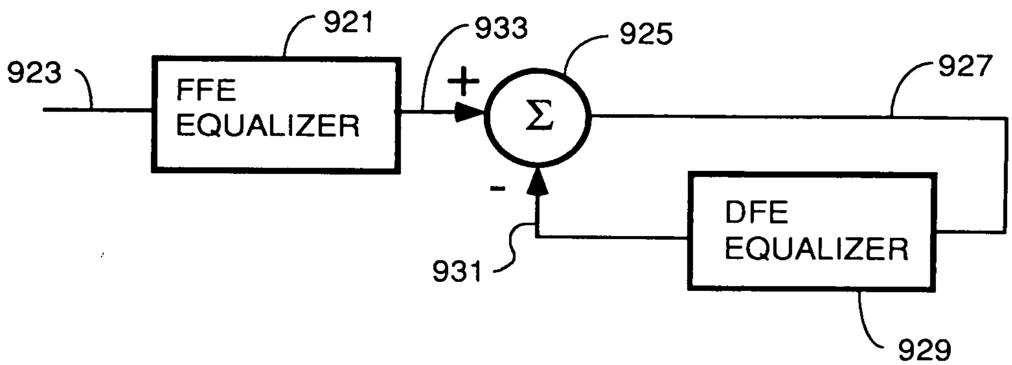


FIG. 50

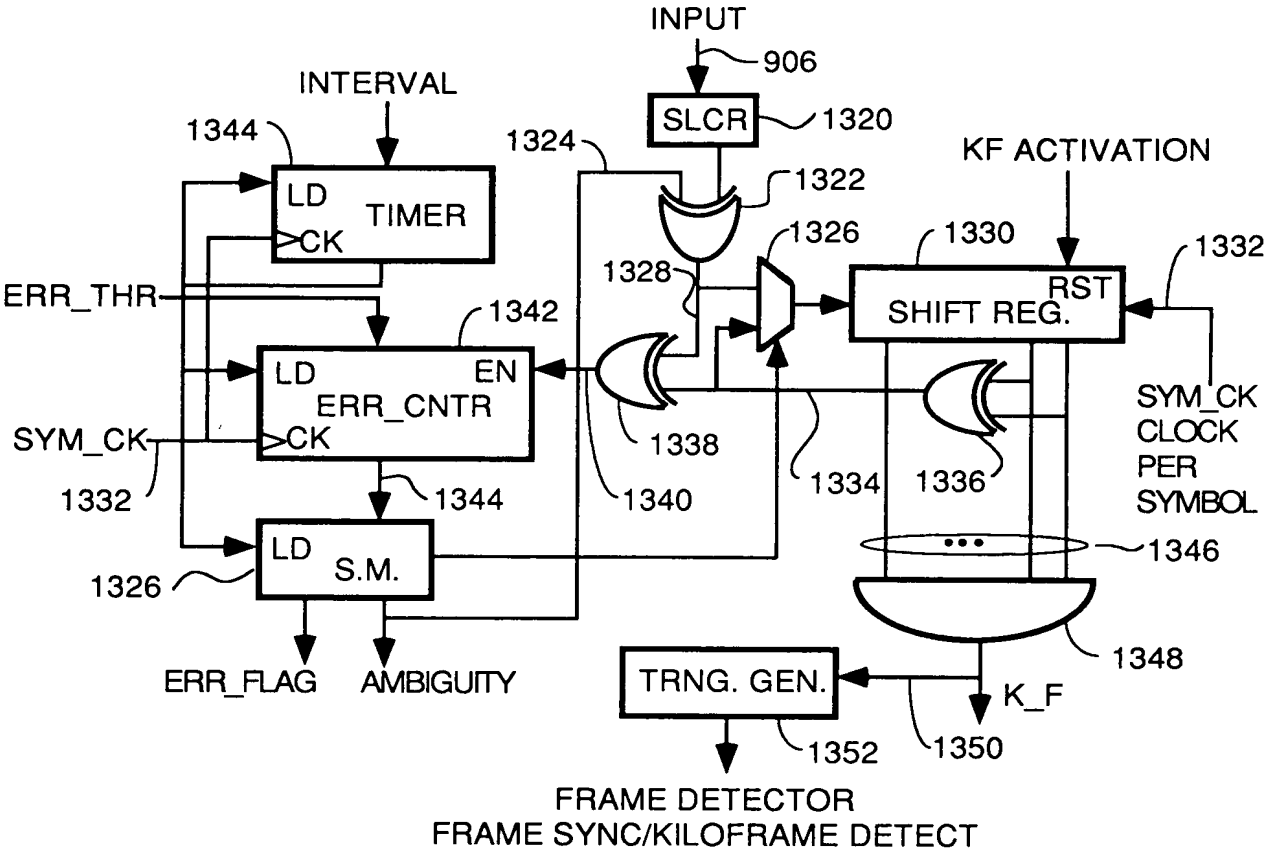
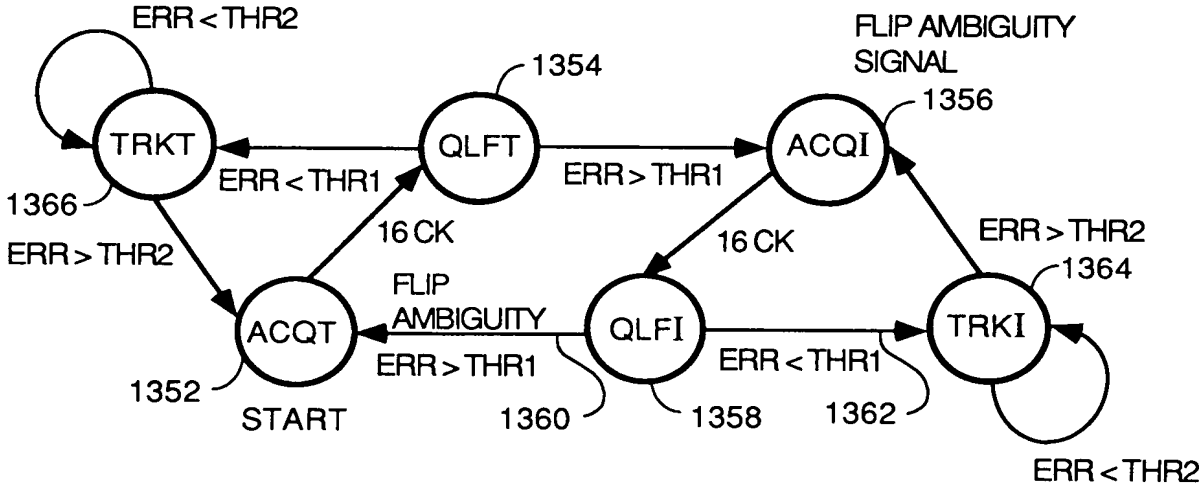


FIG. 51



STATE MACHINE

FIG. 52

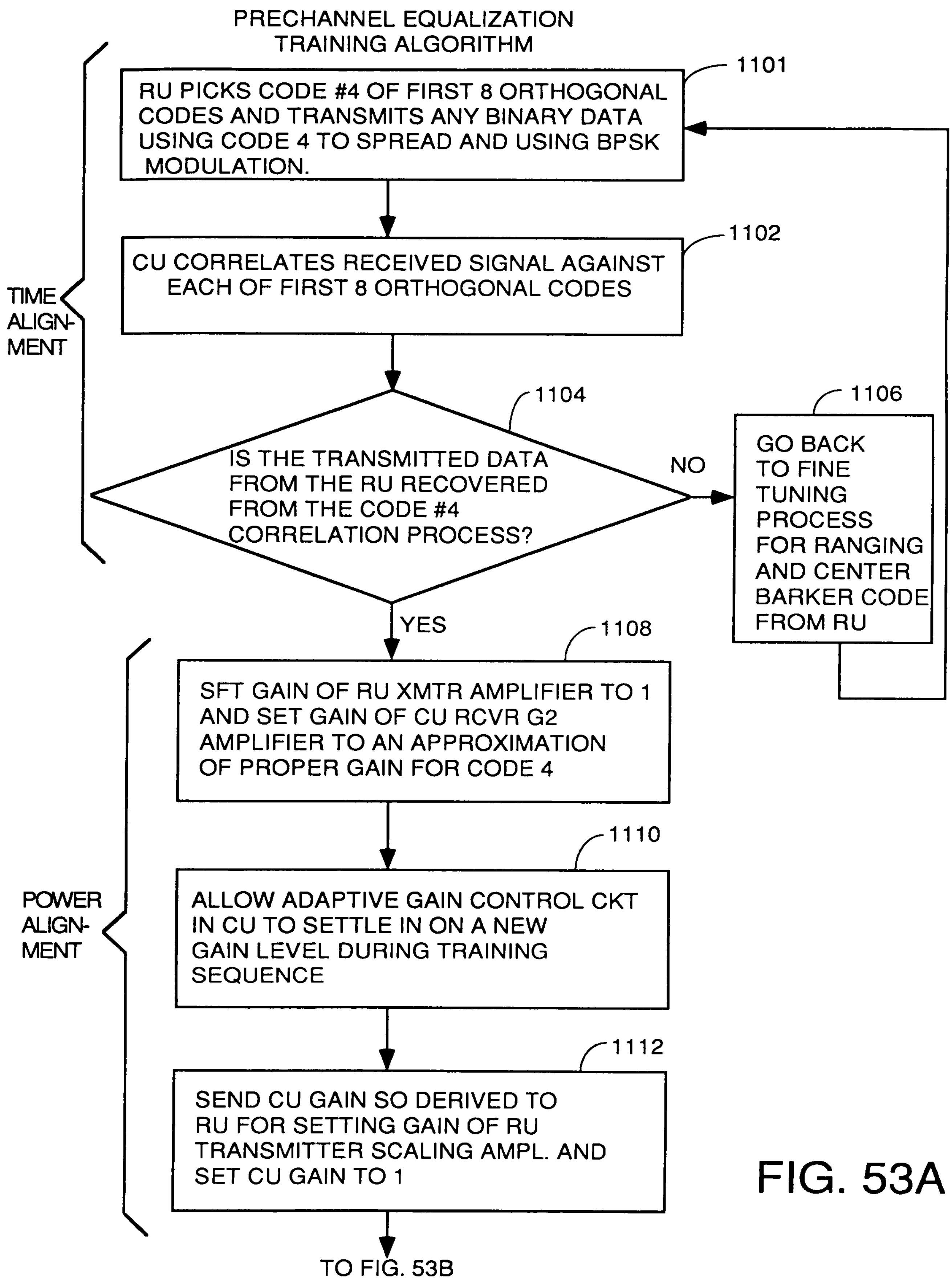

PRECHANNEL EQUALIZATION TRAINING ALGORITHM
TIME ALIGNMENT
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1101
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
1102
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
1104
NO
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
1106
YES
POWER ALIGNMENT
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
1108
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1110
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
1112
TO FIG. 53B

FIG. 53A

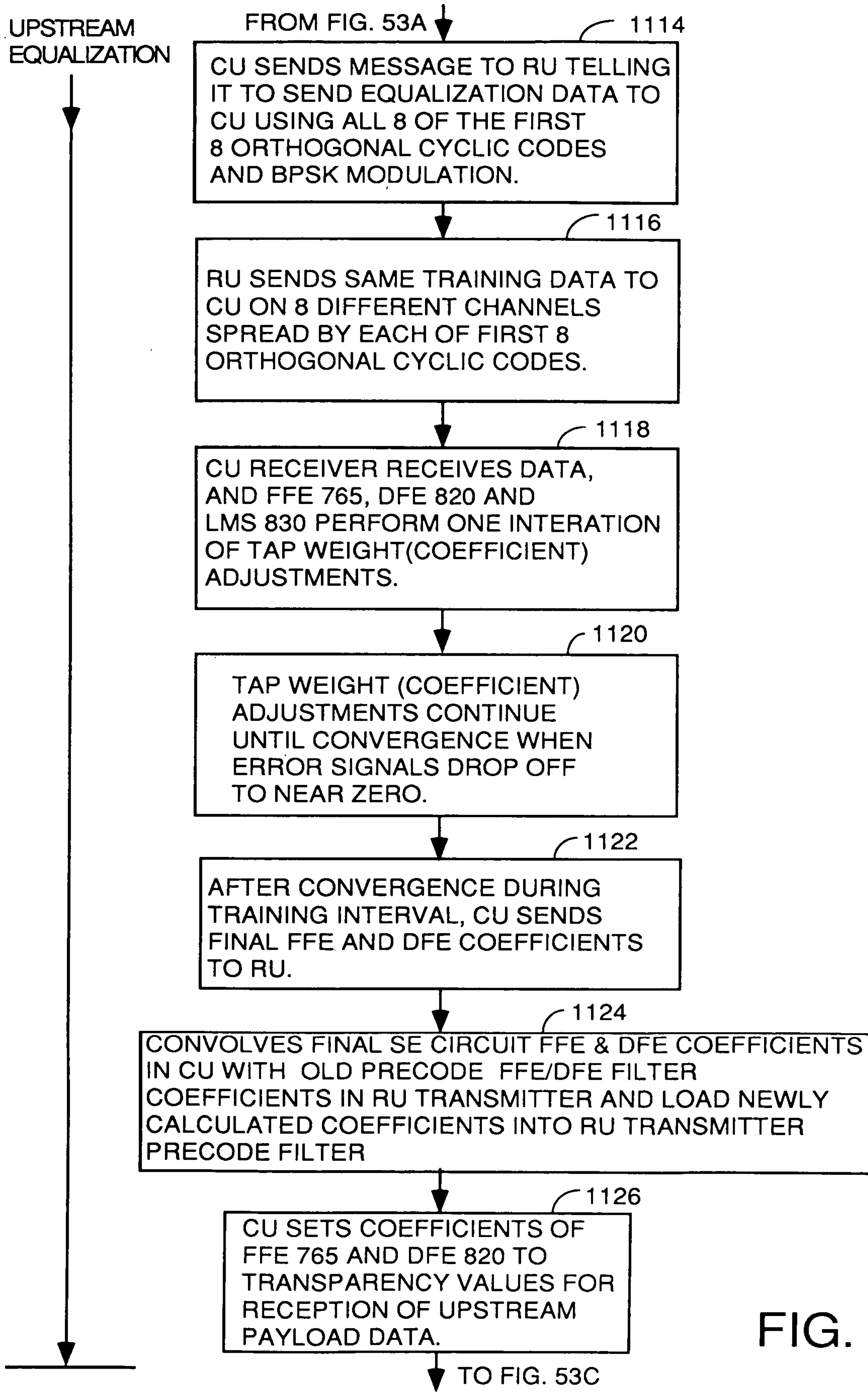

UPSTREAM EQUALIZATION
FROM FIG. 53A
1114
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
1124
CONVOLVES FINAL SE CIRCUIT FFE & DFE COEFFICIENTS IN CU WITH OLD PRECODE FFE/DFE FILTER COEFFICIENTS IN RU TRANSMITTER AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU TRANSMITTER PRECODE FILTER
1126
CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO TRANSPARENCY VALUES FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
TO FIG. 53C

FIG. 53B

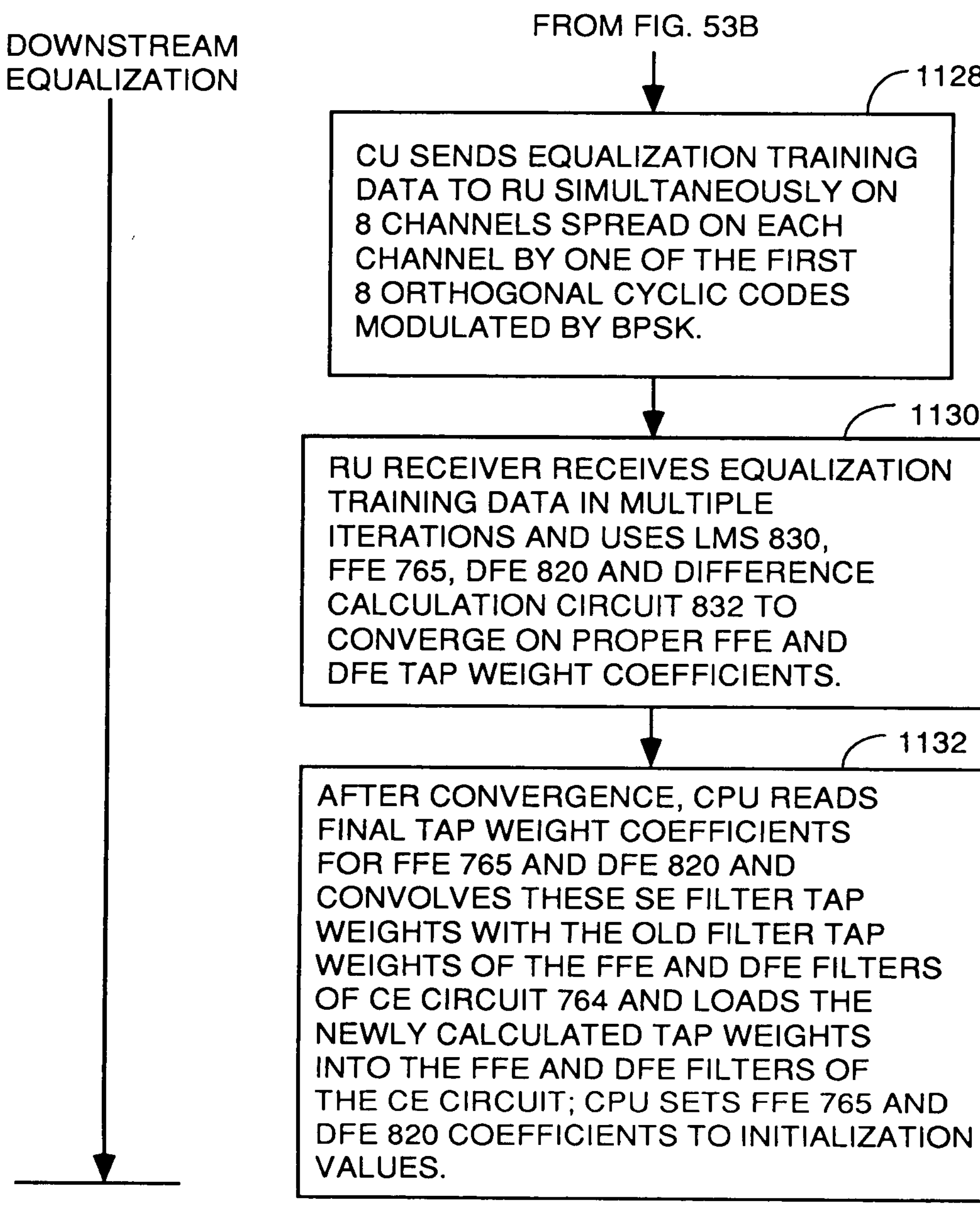


FIG. 53C

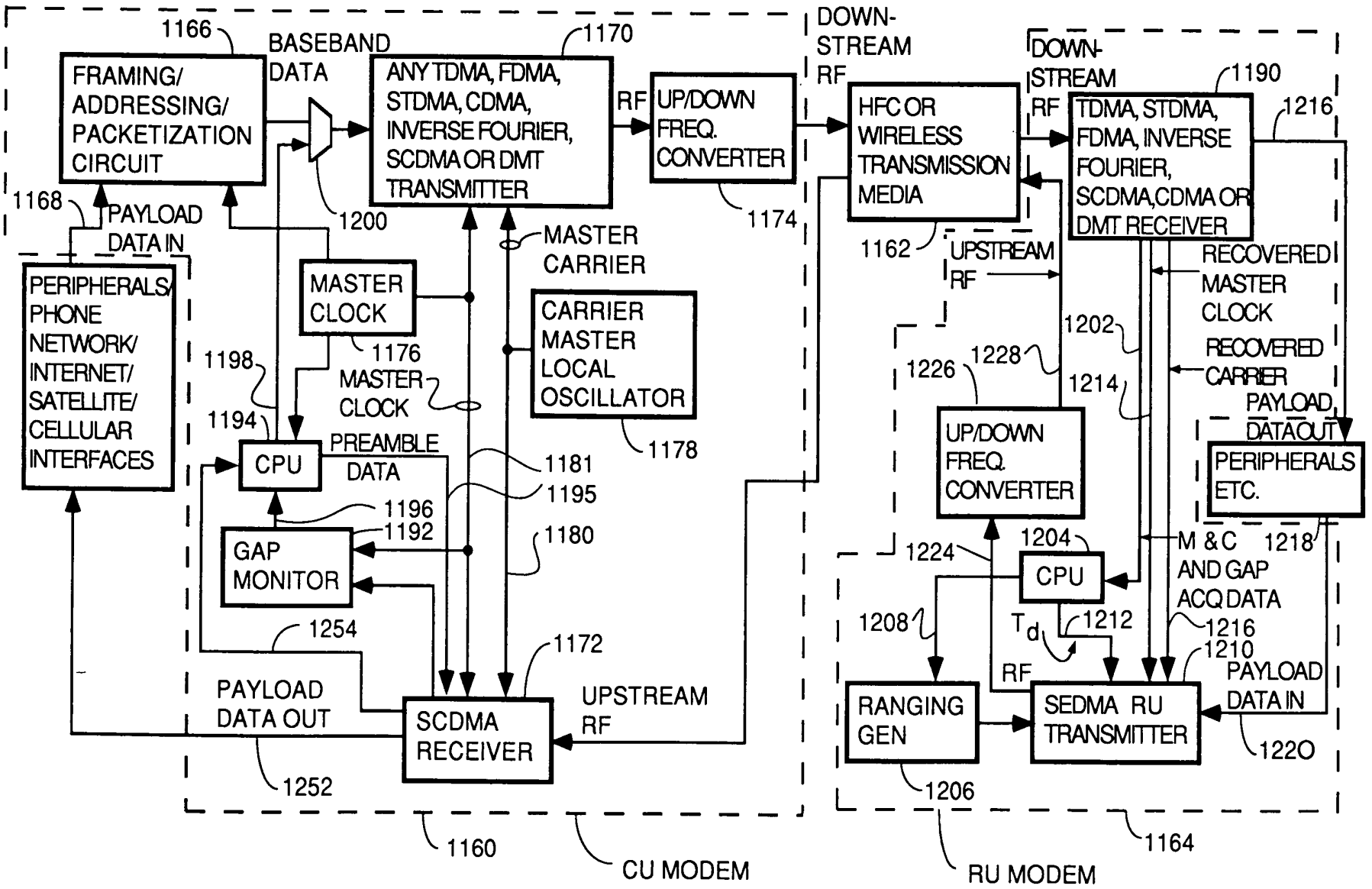
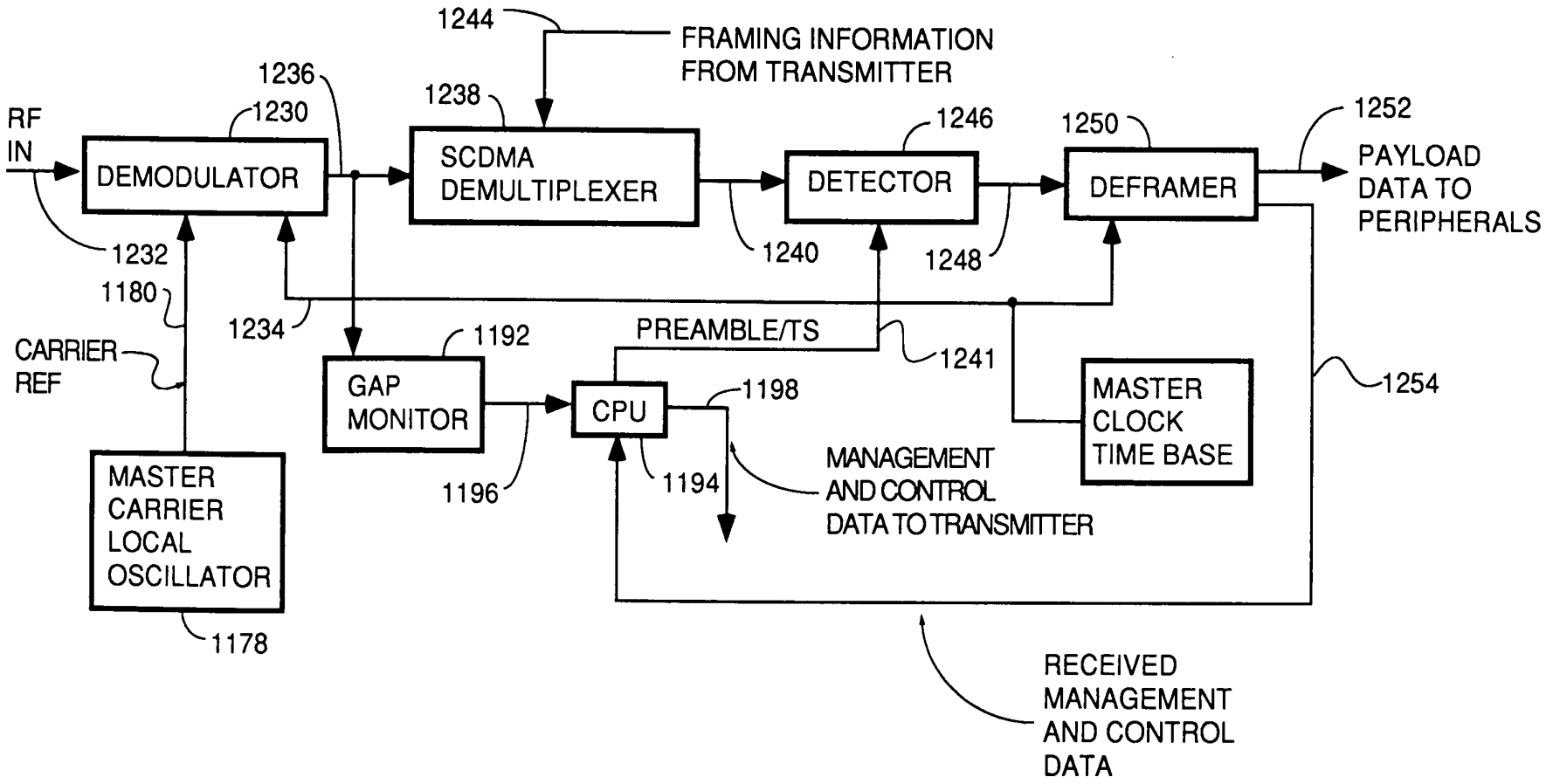
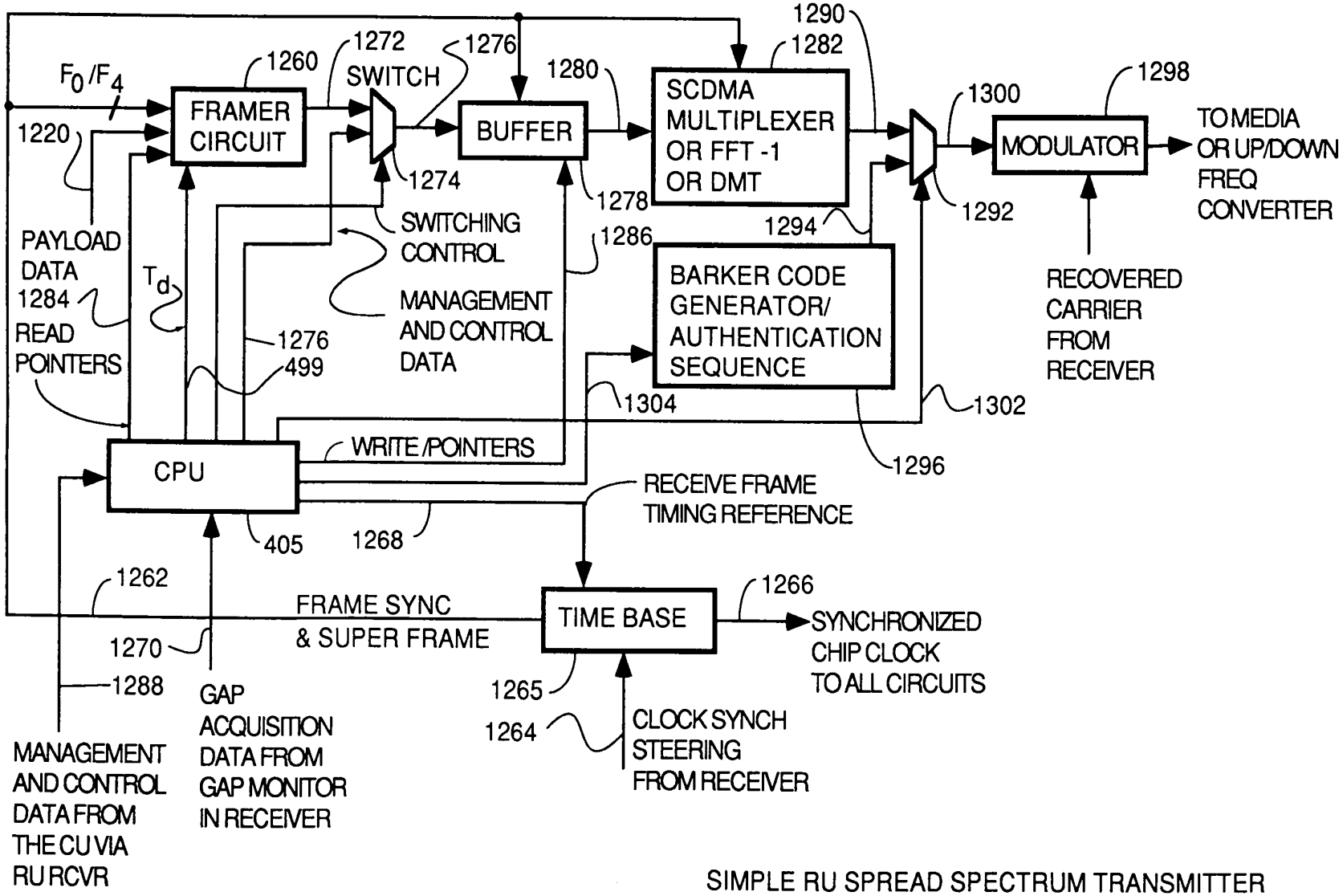


FIG. 54



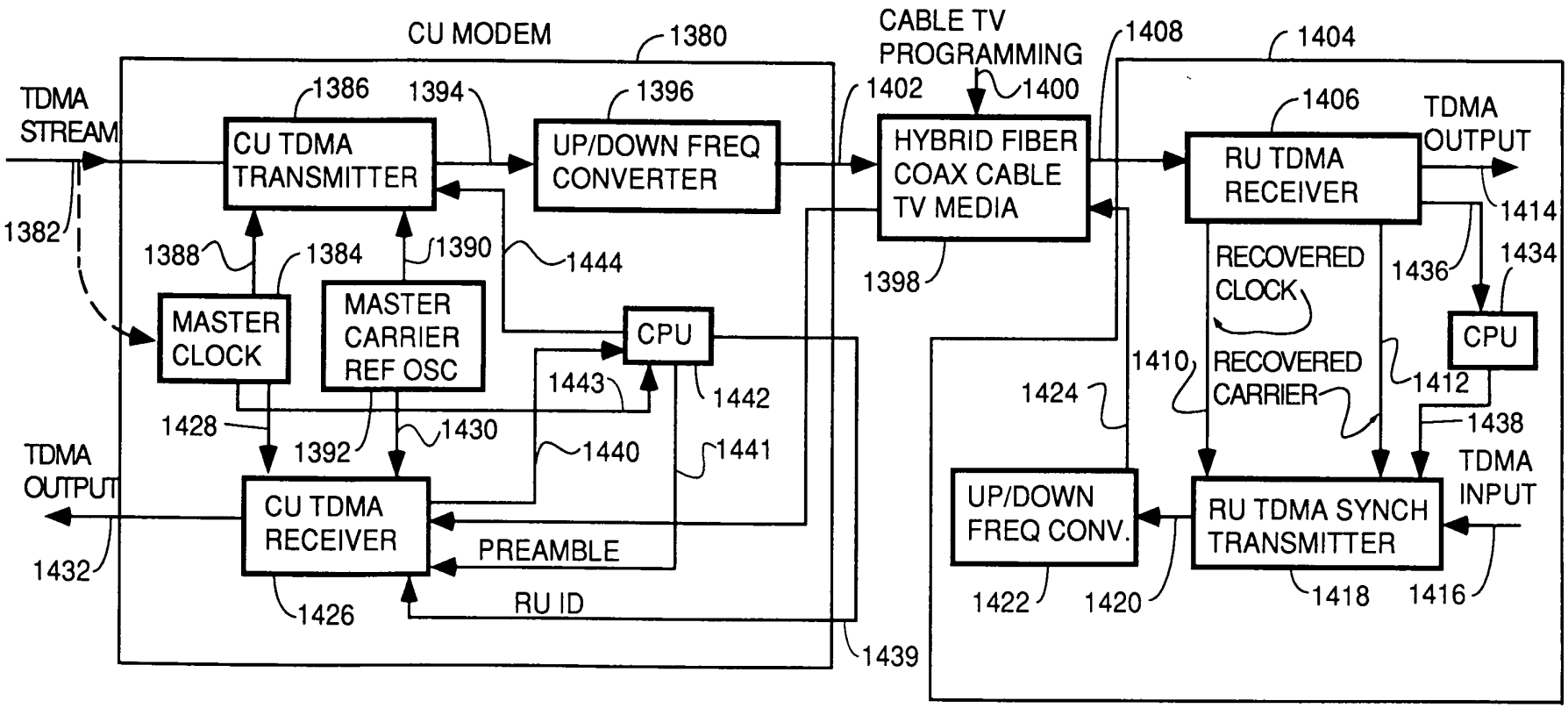
SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55



SIMPLE RU SPREAD SPECTRUM TRANSMITTER

FIG. 56



SYNCHRONOUS TDMA SYSTEM

FIG. 57

OFFSET	1B ASIC		2A ASIC	
(CHIPS)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

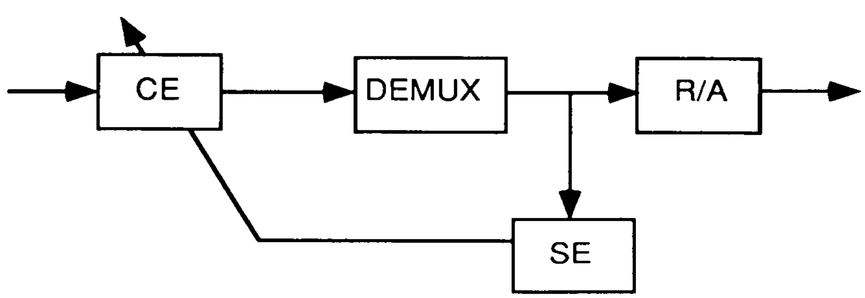
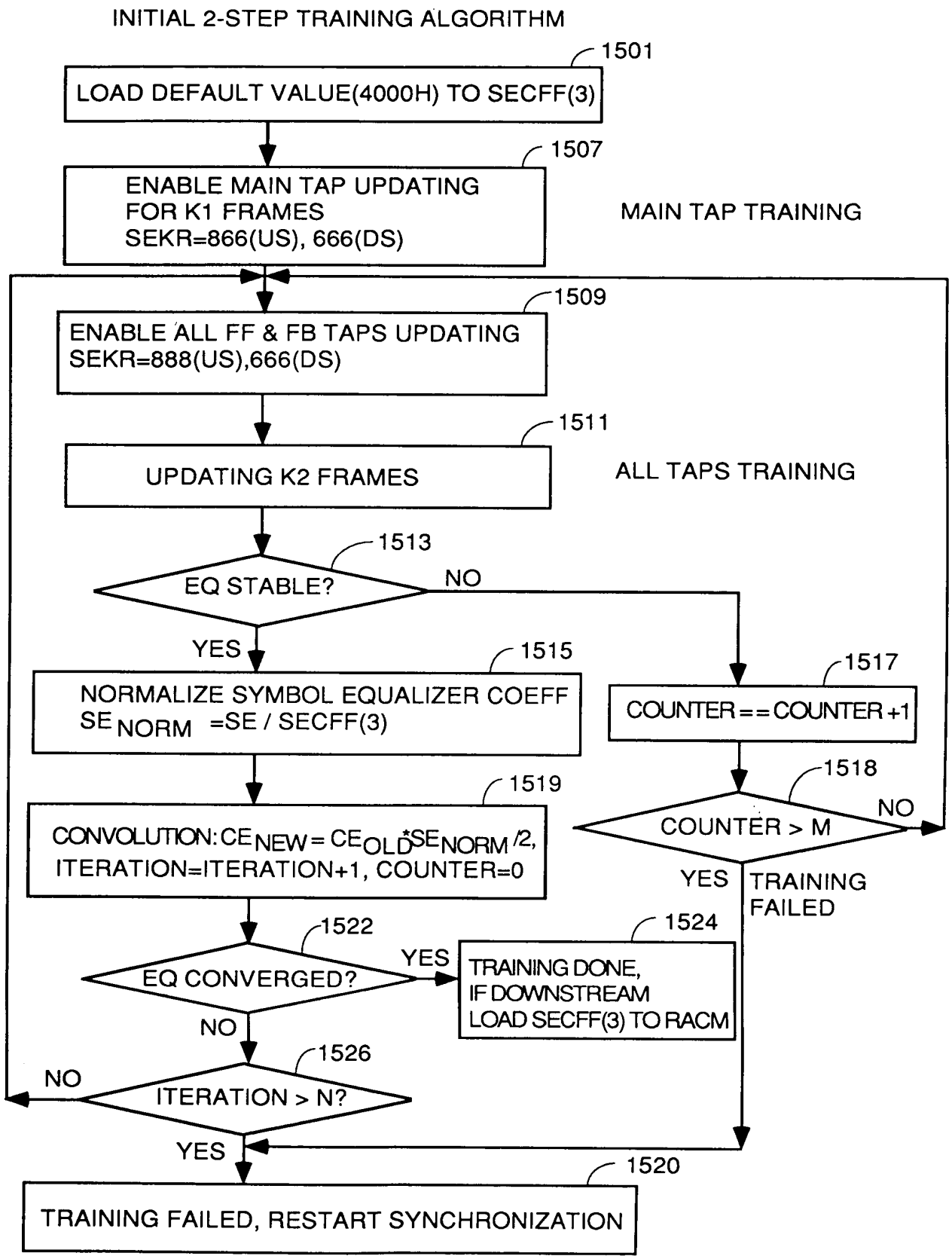


FIG. 59



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

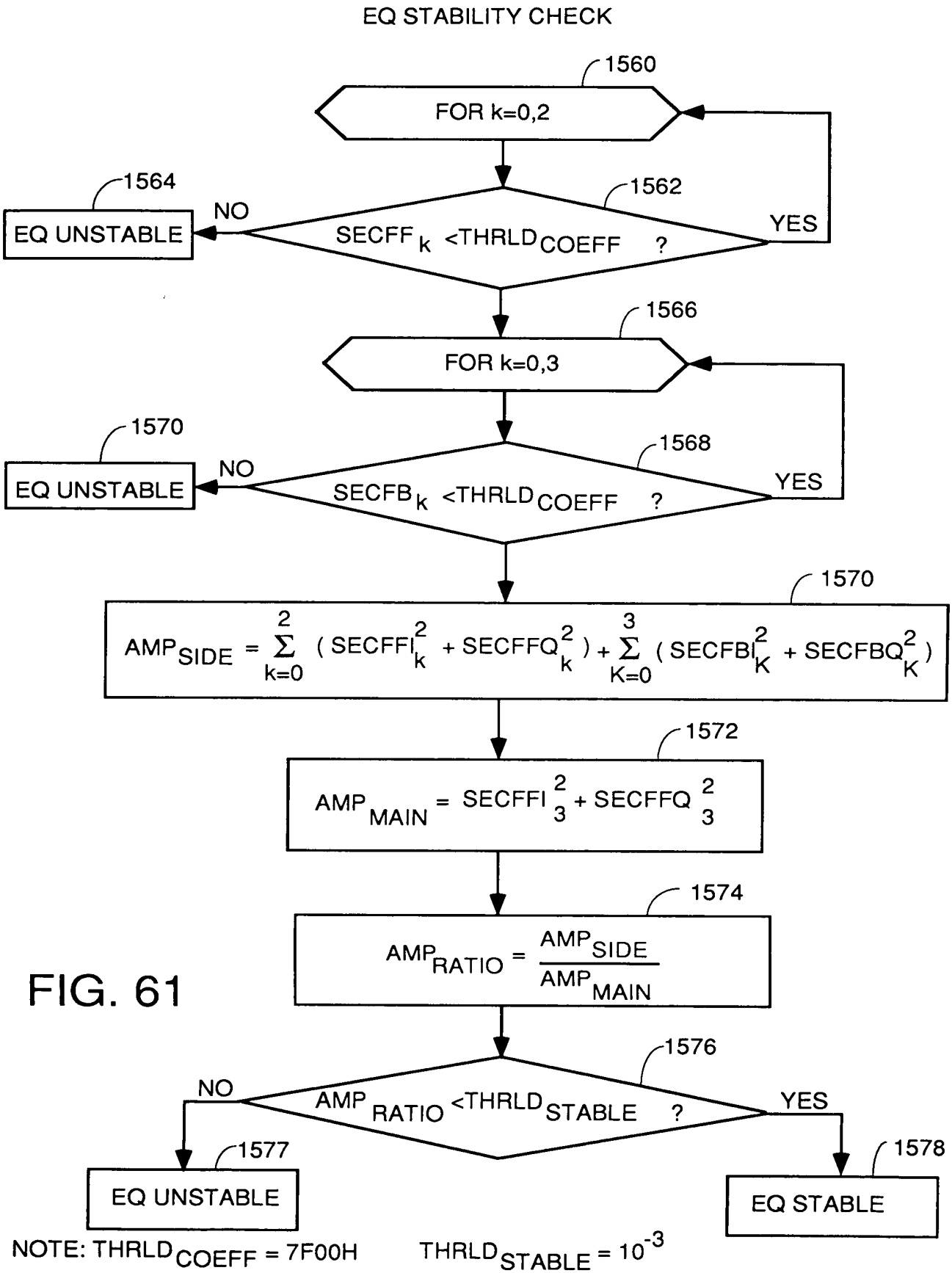
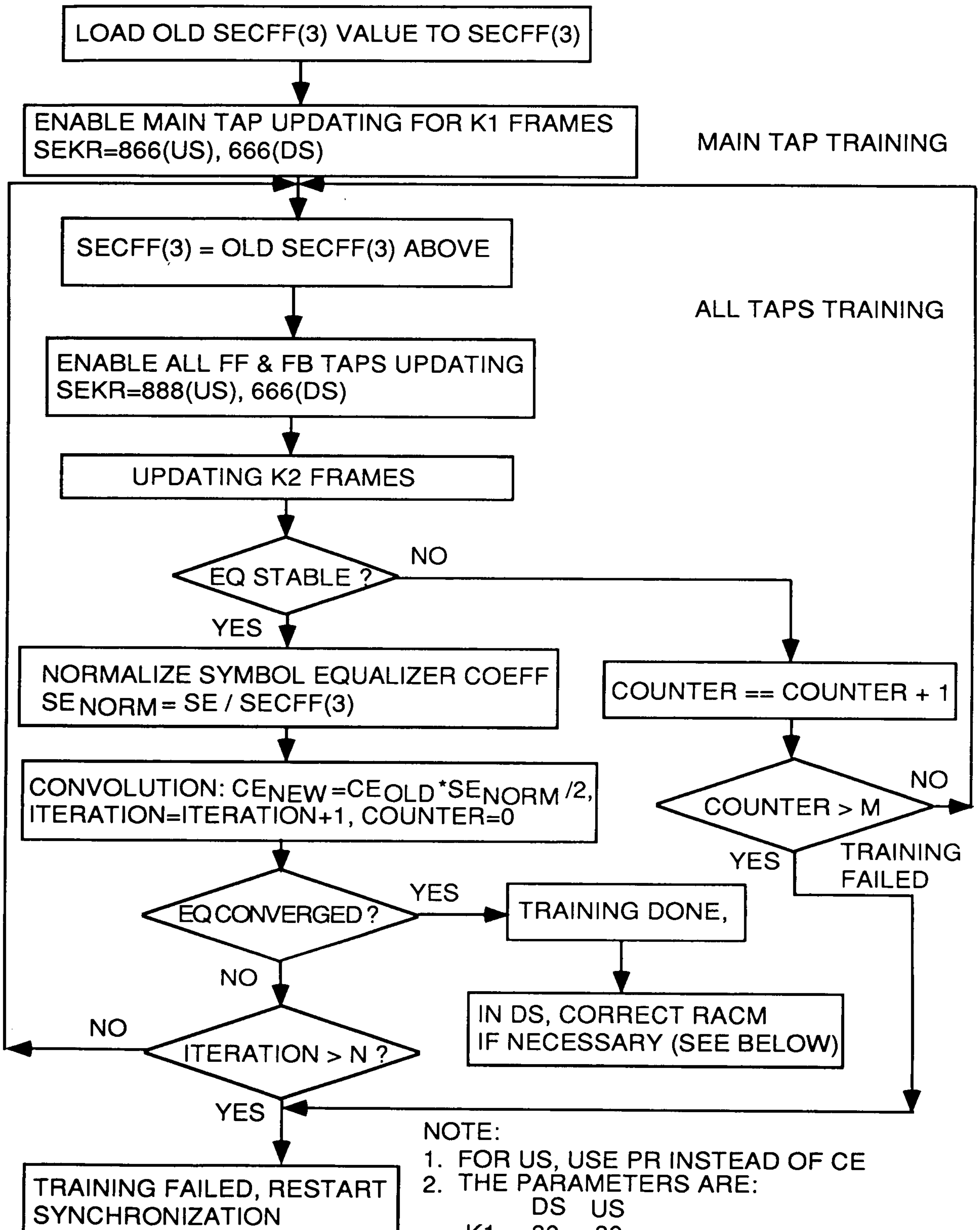

EQ STABILITY CHECK
1560
FOR k=0,2
1562
SECFF k <THRLD COEFF ?
NO
YES
1564
EQ UNSTABLE
1566
FOR k=0,3
1568
SECFB k <THRLD COEFF ?
NO
YES
1570
EQ UNSTABLE
1570
AMP SIDE = Σ k=0 2 (SECFFI k 2 + SECFFQ k 2) + Σ K=0 3 (SECFBI K 2 + SECFBQ K 2)
1572
AMP MAIN = SECFFI 3 2 + SECFFQ 3 2
1574
AMP RATIO = AMP SIDE / AMP MAIN
1576
AMP RATIO <THRLD STABLE ?
NO
YES
1577
EQ UNSTABLE
1578
EQ STABLE
NOTE: THRLD COEFF = 7F00H
THRLD STABLE = 10-3

FIG. 61

PERIODIC 2-STEP TRAINING ALGORITHM


LOAD OLD SECFF(3) VALUE TO SECFF(3)
ENABLE MAIN TAP UPDATING FOR K1 FRAMES
SEKR=866(US), 666(DS)
MAIN TAP TRAINING
SECFF(3) = OLD SECFF(3) ABOVE
ALL TAPS TRAINING
ENABLE ALL FF & FB TAPS UPDATING
SEKR=888(US), 666(DS)
UPDATING K2 FRAMES
EQ STABLE ?
NO
YES
NORMALIZE SYMBOL EQUALIZER COEFF
SE NORM = SE / SECFF(3)
COUNTER == COUNTER + 1
CONVOLUTION: CE NEW =CE OLD *SE NORM /2,
ITERATION=ITERATION+1, COUNTER=0
COUNTER > M
NO
YES
TRAINING
FAILED
EQ CONVERGED ?
YES
TRAINING DONE,
NO
IN DS, CORRECT RACM
IF NECESSARY (SEE BELOW)
NO
ITERATION > N ?
YES
TRAINING FAILED, RESTART
SYNCHRONIZATION

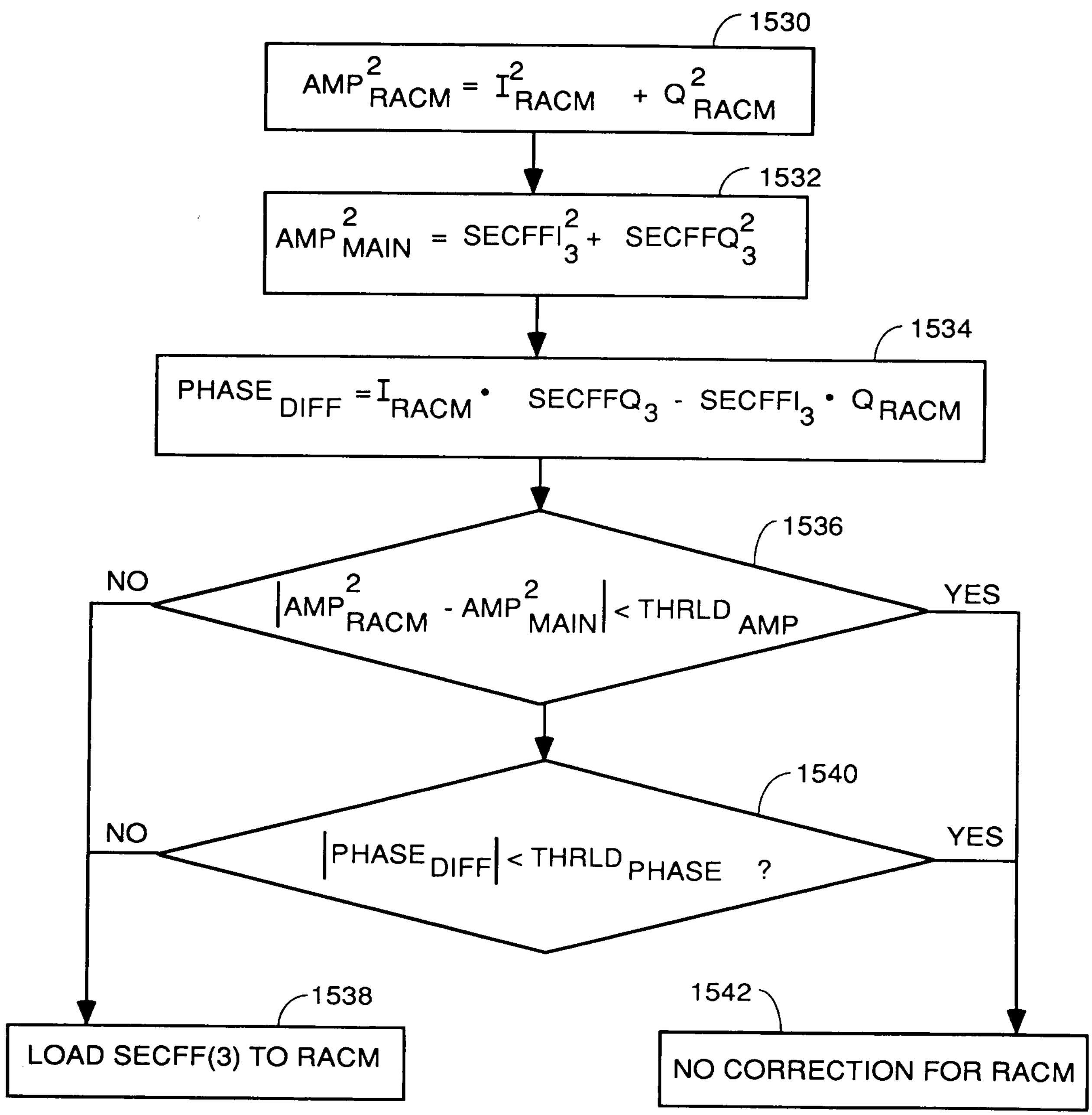
NOTE:

1. FOR US, USE PR INSTEAD OF CE
2. THE PARAMETERS ARE:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM CORRECTION



NOTE: $THRLD_{AMP}$ = TBD

$THRLD_{PHASE}$ = TBD

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

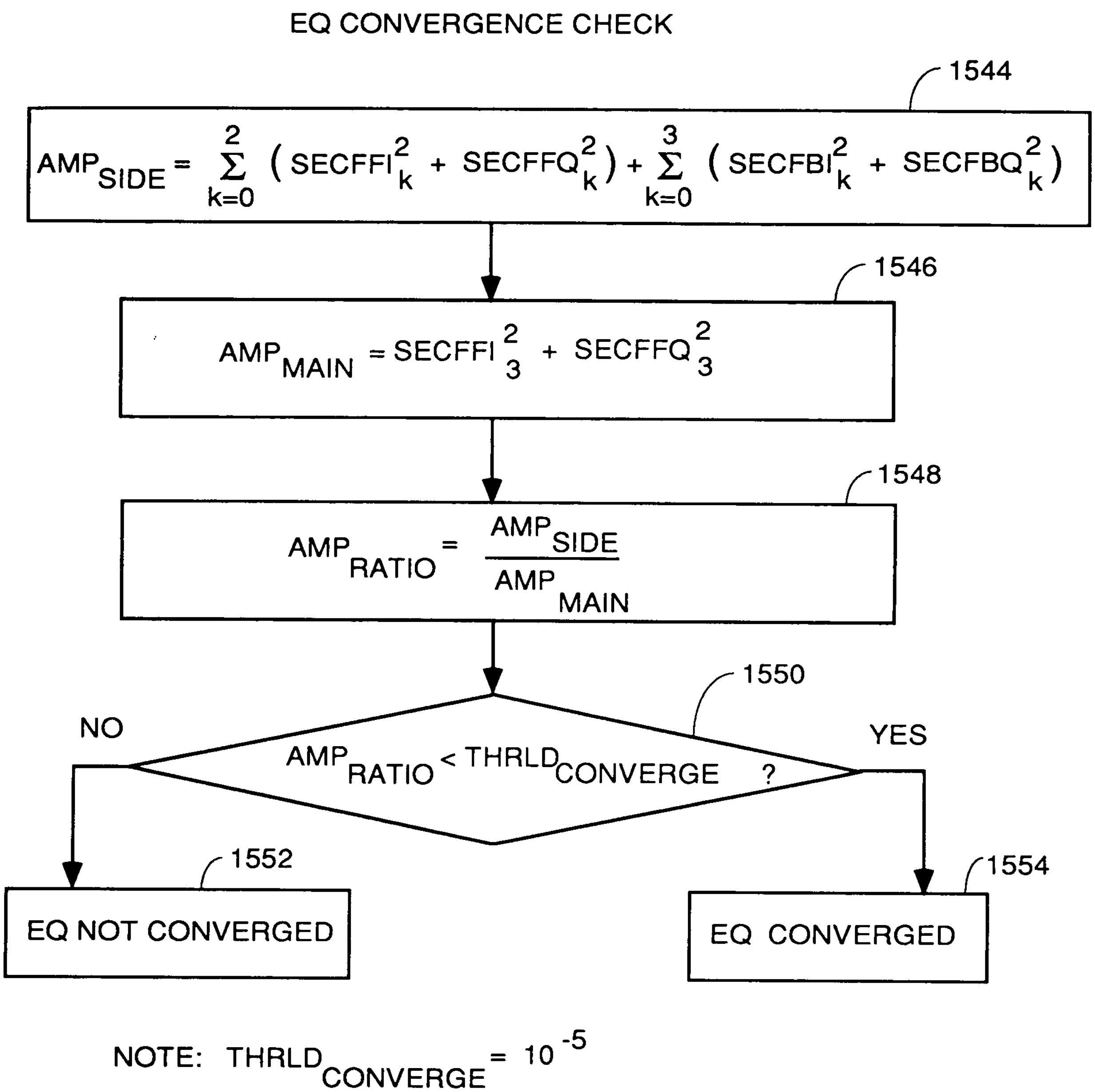
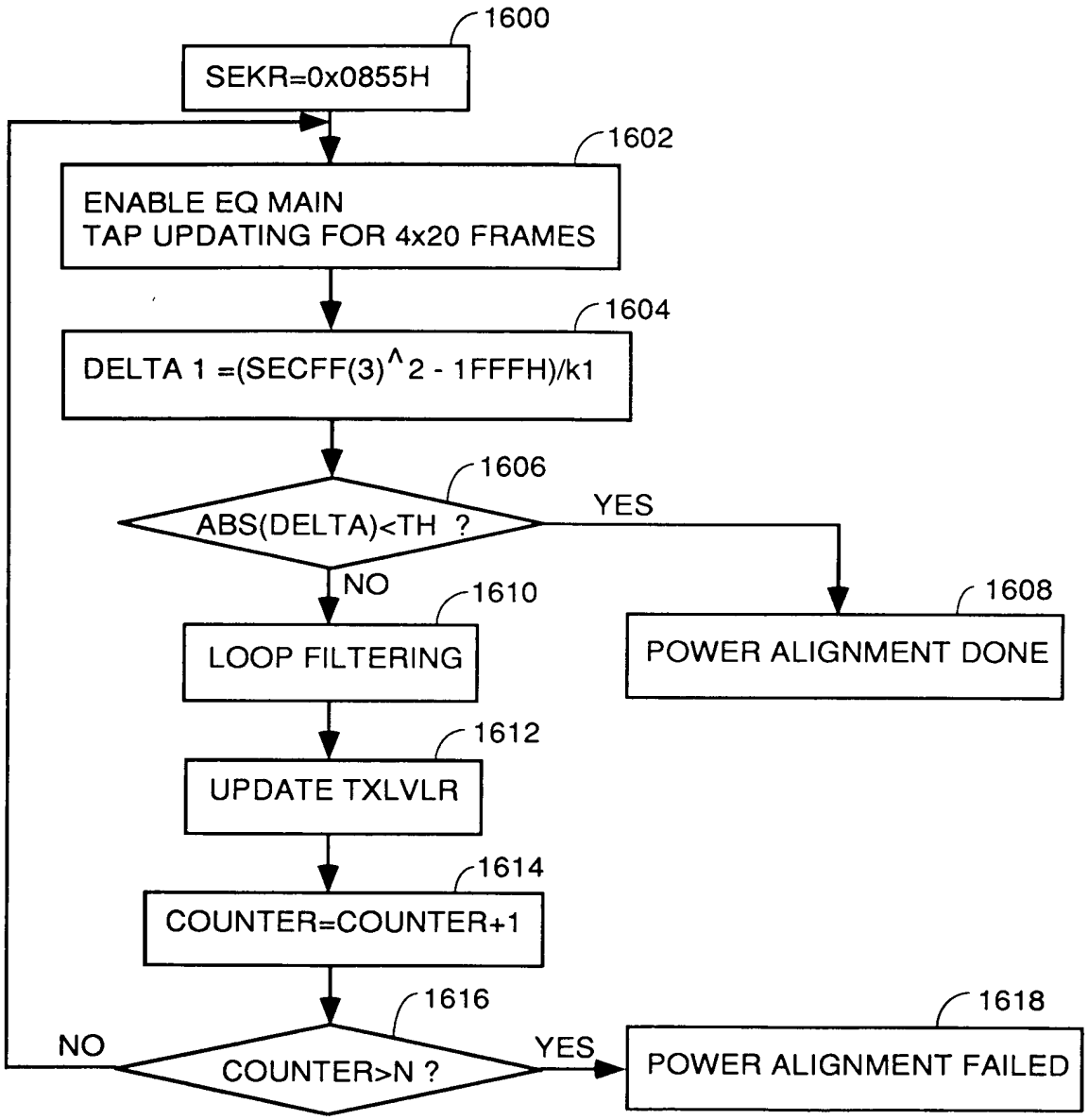


FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H

N = 12

FIG. 65

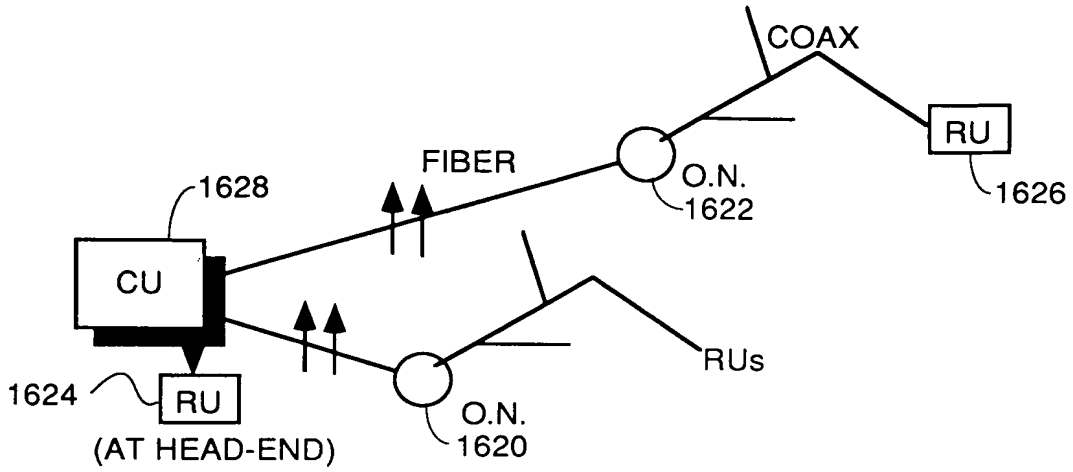
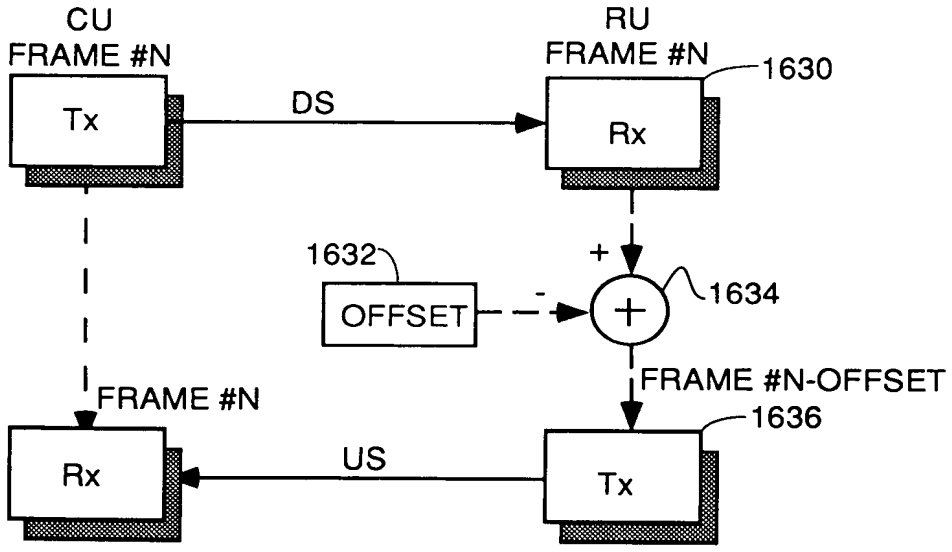


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

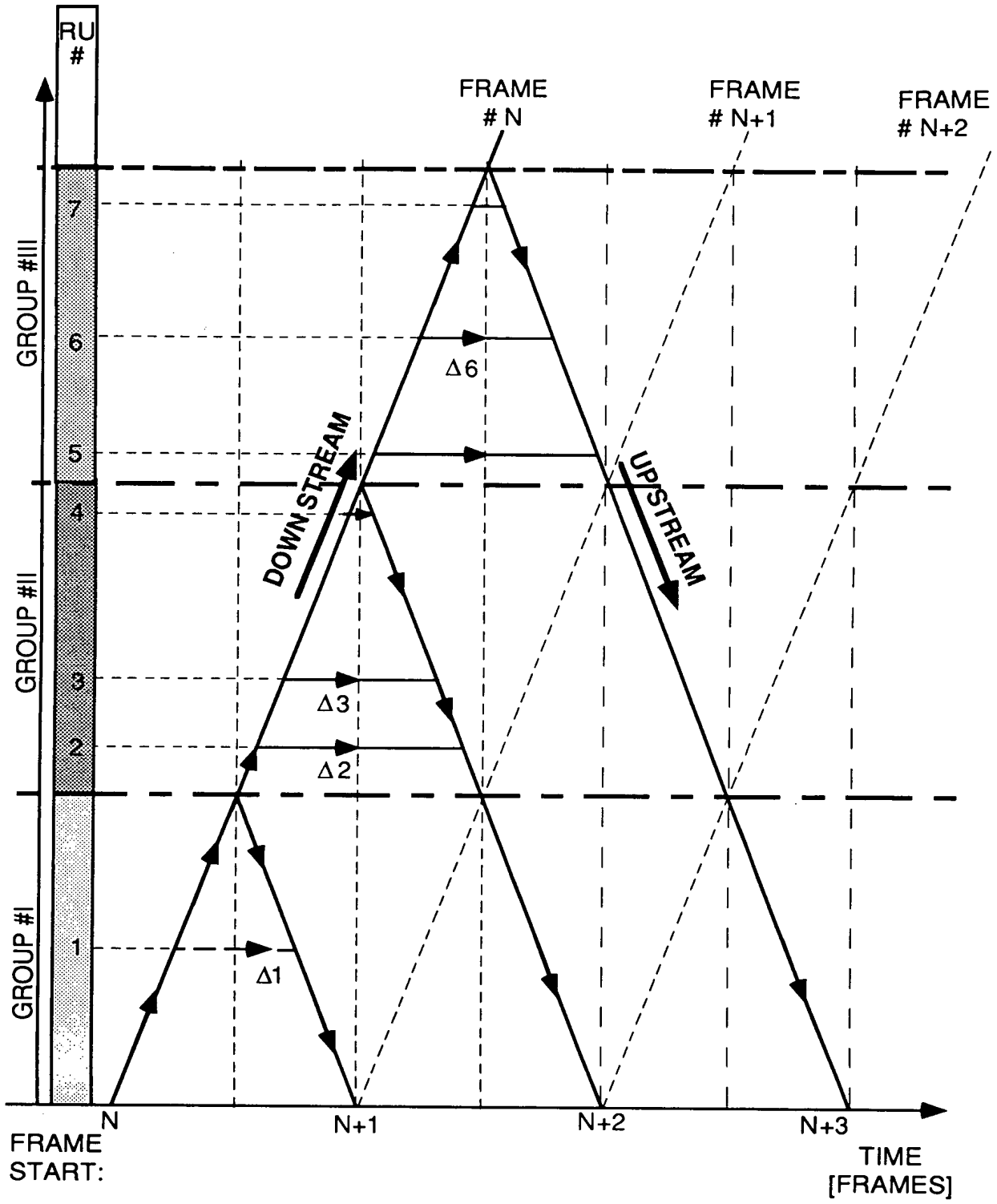
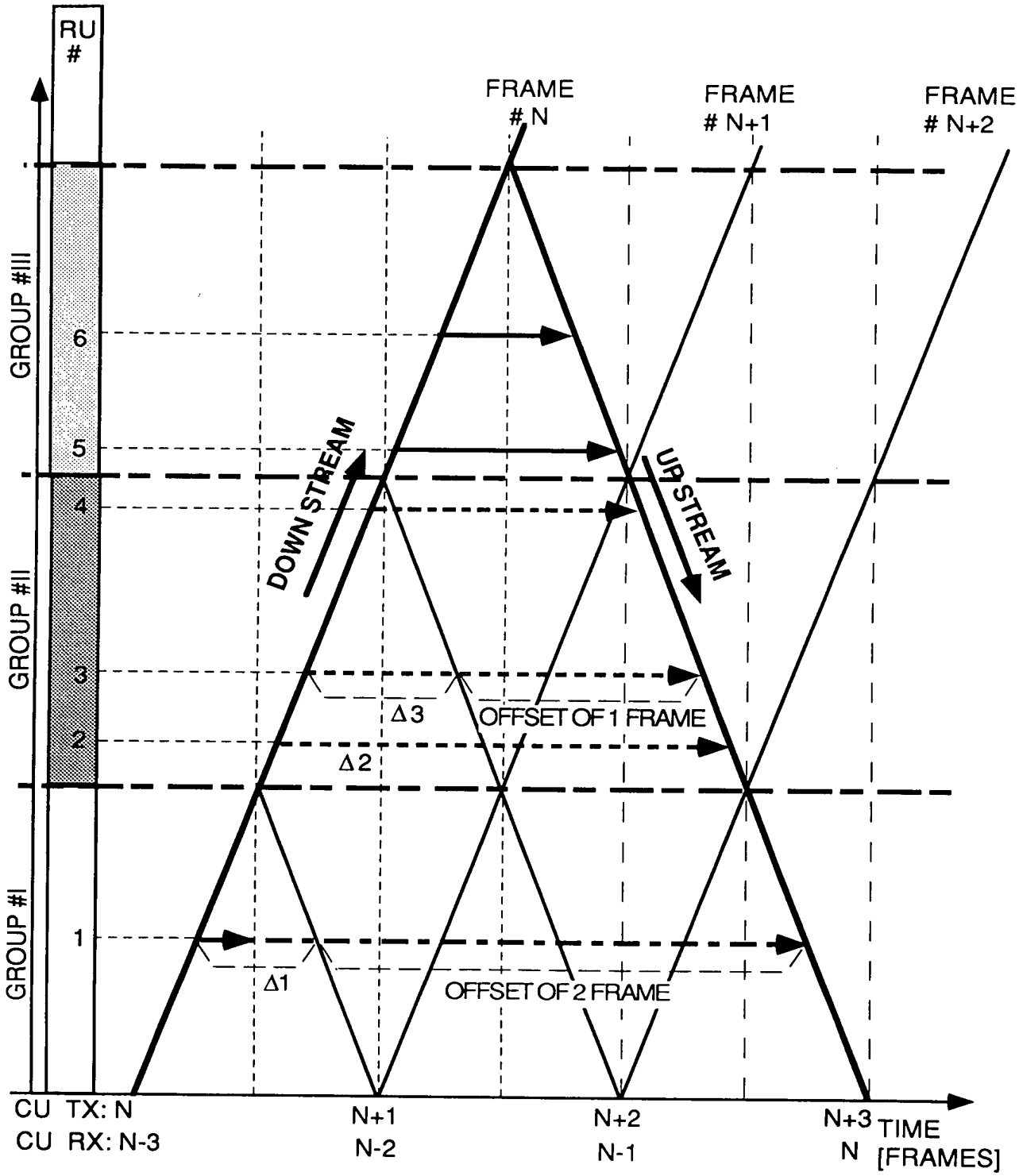


FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM) PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

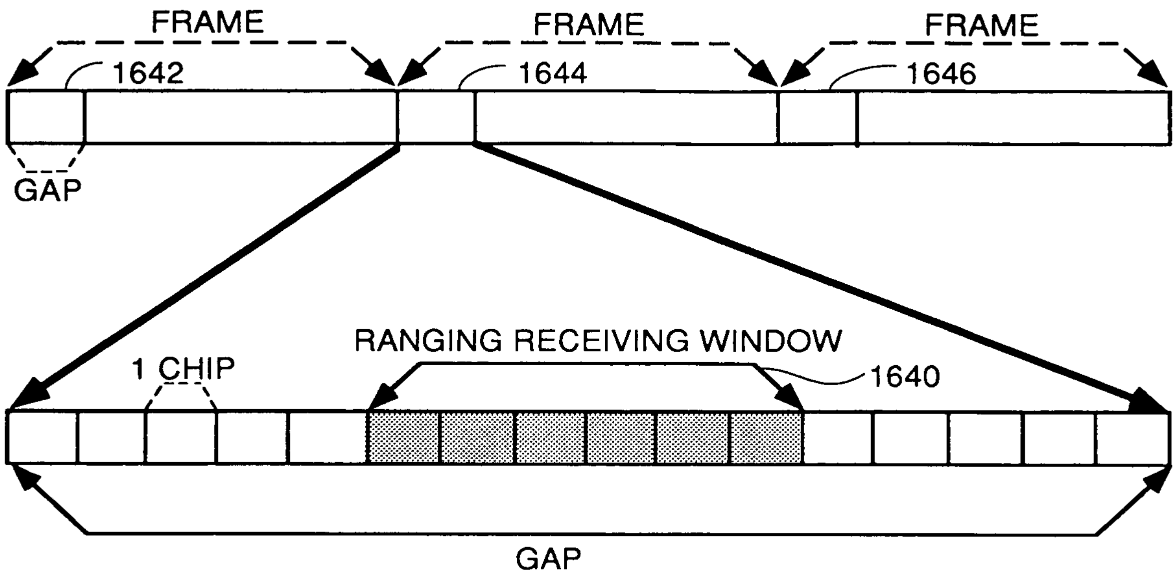
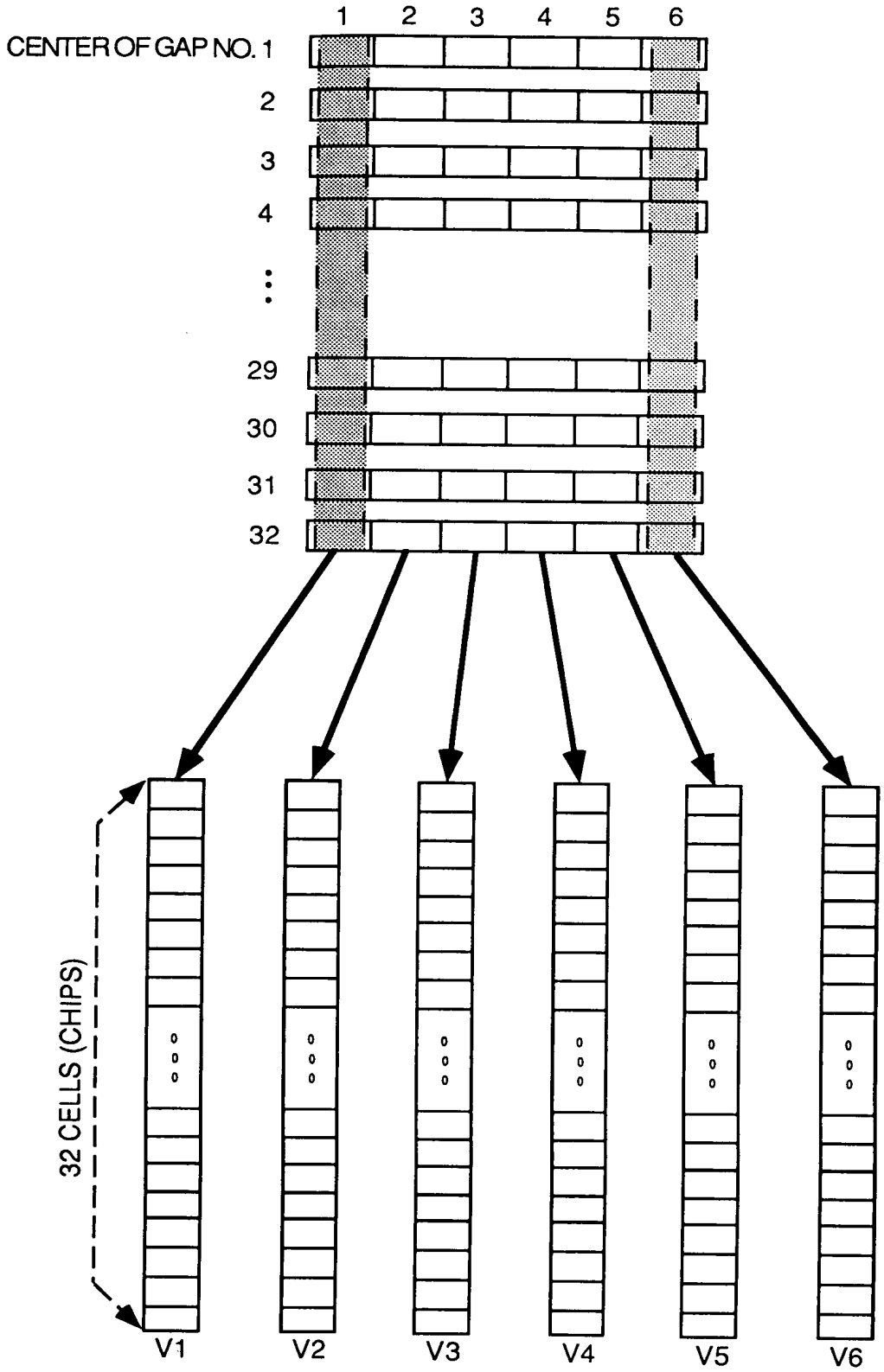

FRAME
FRAME
FRAME
1642
1644
1646
GAP
RANGING RECEIVING WINDOW
1 CHIP
1640
GAP

FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	•••	0
2	1	0	0	1	1	1	1	•••	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	•••	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	•••	

FIG. 72